LPC11C12/C14

32-bit ARM Cortex-M0 microcontroller; 16/32 kB flash, 8 kB SRAM; C_CAN

Rev. 00.05 — 23 April 2010 Preliminary data sheet

1. General description

The LPC11C12/C14 are an ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11C12/C14 operate at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC11C12/C14 includes 16/32 kB of flash memory, 8 kB of data memory, one C_CAN controller, one Fast-mode Plus I^{2}C-bus interface, one RS-485/EIA-485 UART, two SPI interfaces with SSP features, four general purpose counter/timers, a 10-bit ADC, and 40 general purpose I/O pins.

On-chip C_CAN drivers and flash In-System Programming tools via C_CAN are included.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug.
  - System tick timer.
- Memory:
  - 32 kB (LPC11C14) or 16 kB (LPC11C12) on-chip flash programming memory.
  - 8 kB SRAM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
  - Flash ISP commands can be issued via UART or C_CAN.
- Digital peripherals:
  - 40 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current output driver (20 mA) on one pin.
  - High-current sink drivers (20 mA) on two I^{2}C-bus pins in Fast-mode Plus.
  - Four general purpose counter/timers with a total of four capture inputs and 13 match outputs.
  - Programmable WatchDog Timer (WDT).
- Analog peripherals:
  - 10-bit ADC with input multiplexing among 8 pins.

- Serial interfaces:
  - UART with fractional baud rate generation, internal FIFO, and RS-485 support.
  - Two SPI controllers with SSP features and with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
  - C_CAN controller. On-chip C_CAN drivers included.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 7.8 kHz to 1.8 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator, IRC, CPU clock, or the Watchdog clock.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using 13 of the GPIO pins.
  - Power-On Reset (POR).
  - Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Available as 48-pin LQFP package.

3. Applications

- eMetering
- Elevator systems
- Industrial and sensor based networks
- White goods

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11C12FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	sot313-2
LPC11C14FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	sot313-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	Total SRAM	UART RS-485	I²C/ Fast+	SPI	C_CAN	ADC channels	Package
LPC11C12FBD48/301	16 kB	8 kB	1	1	2	1	8	LQFP48
LPC11C14FBD48/301	32 kB	8 kB	1	1	2	1	8	LQFP48

5. Block diagram

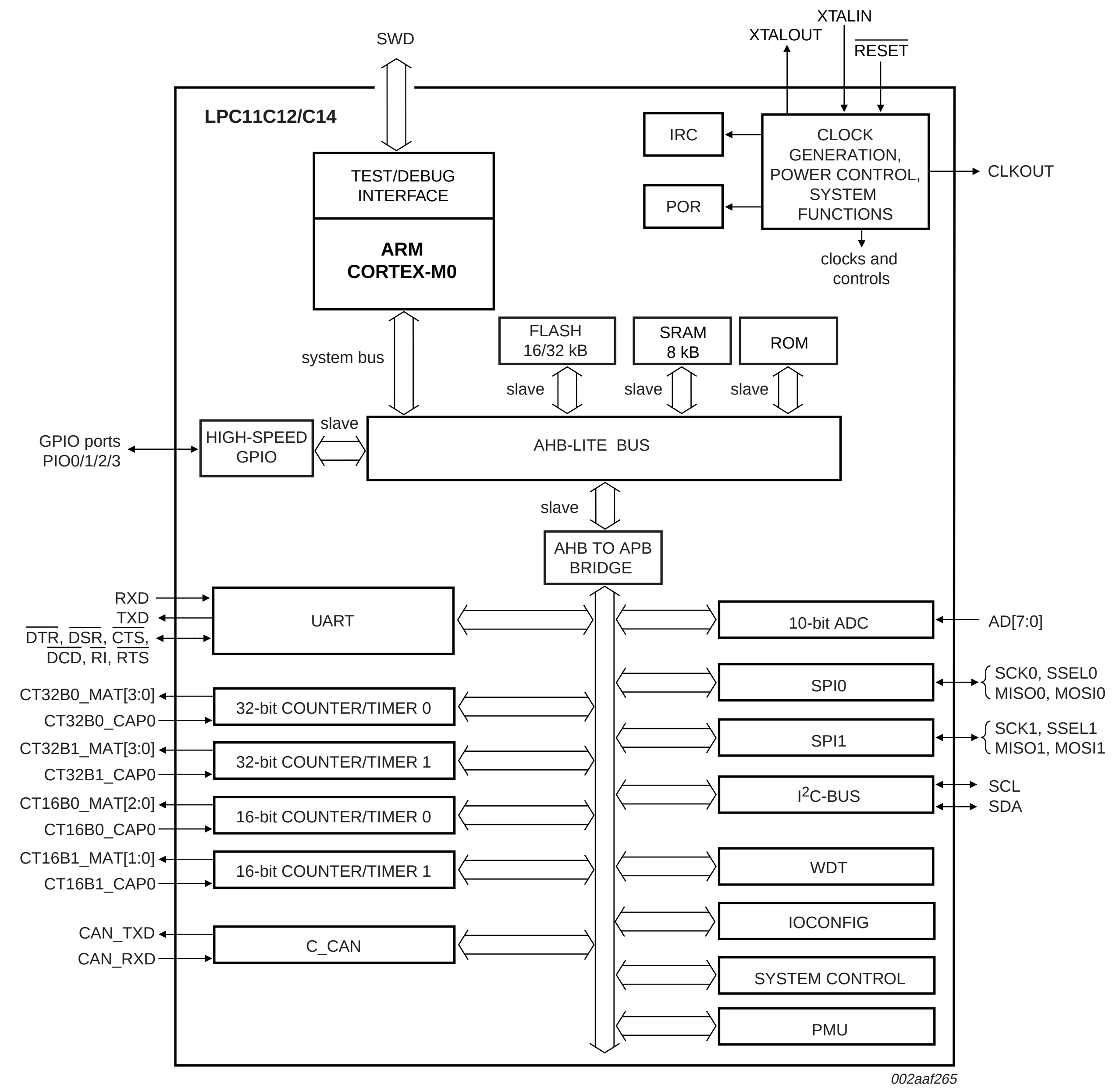


Fig 1. LPC11C12/C14 block diagram

6. Pinning information

6.1 Pinning

Fig 2. Pin configuration LQFP48 package

6.2 Pin description

Table 3. LPC11C14 pin description table (LQFP48 package)

Symbol	Pin	Type	Description
PIO0_0 to PIO0_11		I/O	**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	3[1]	I	**RESET —** External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
		I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	4[2]	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the flash ISP command handler via UART (if PIO0_3 is HIGH) or via C_CAN (if PIO0_3 is LOW).
		O	**CLKOUT —** Clockout pin.
		O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	10[2]	I/O	**PIO0_2 —** General purpose digital input/output pin.
		O	**SSEL0 —** Slave Select for SPI0.
		I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	14[2]	I/O	**PIO0_3 —** General purpose digital input/output pin. This pin is monitored during reset: Together with a LOW level on pin PIO0_1, a LOW level starts the flash ISP command handler via C_CAN and a HIGH level starts the flash ISP command handler via UART.
PIO0_4/SCL	15[3]	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
		I/O	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[3]	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
		I/O	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	22[2]	I/O	**PIO0_6 —** General purpose digital input/output pin.
		I/O	**SCK0 —** Serial clock for SPI0.
PIO0_7/CTS	23[2]	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
		I	**CTS —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27[2]	I/O	**PIO0_8 —** General purpose digital input/output pin.
		I/O	**MISO0 —** Master In Slave Out for SPI0.
		O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28[2]	I/O	**PIO0_9 —** General purpose digital input/output pin.
		I/O	**MOSI0 —** Master Out Slave In for SPI0.
		O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/CT16B0_MAT2	29[2]	I	**SWCLK —** Serial wire clock.
		I/O	**PIO0_10 —** General purpose digital input/output pin.
		I/O	**SCK0 —** Serial clock for SPI0.
		O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.

Table 3. LPC11C14 pin description table (LQFP48 package) *…continued*

Symbol	Pin	Type	Description
R/PIO0_11/ AD0/CT32B0_MAT3	32[4]	I	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
		I/O	**PIO0_11 —** General purpose digital input/output pin.
		I	**AD0 —** A/D converter, input 0.
		O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11		I/O	**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33[4]	I	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
		I/O	**PIO1_0 —** General purpose digital input/output pin.
		I	**AD1 —** A/D converter, input 1.
		I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34[4]	O	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
		I/O	**PIO1_1 —** General purpose digital input/output pin.
		I	**AD2 —** A/D converter, input 2.
		O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35[4]	I	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
		I/O	**PIO1_2 —** General purpose digital input/output pin.
		I	**AD3 —** A/D converter, input 3.
		O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/AD4/ CT32B1_MAT2	39[4]	I/O	**SWDIO —** Serial wire debug input/output.
		I/O	**PIO1_3 —** General purpose digital input/output pin.
		I	**AD4 —** A/D converter, input 4.
		O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/WAKEUP	40[4]	I/O	**PIO1_4 —** General purpose digital input/output pin.
		I	**AD5 —** A/D converter, input 5.
		O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
		I	**WAKEUP —** Deep power-down mode wake-up pin. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	45[2]	I/O	**PIO1_5 —** General purpose digital input/output pin.
		O	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
		I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46[2]	I/O	**PIO1_6 —** General purpose digital input/output pin.
		I	**RXD —** Receiver input for UART.
		O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47[2]	I/O	**PIO1_7 —** General purpose digital input/output pin.
		O	**TXD —** Transmitter output for UART.
		O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/CT16B1_CAP0	9[2]	I/O	**PIO1_8 —** General purpose digital input/output pin.
		I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/CT16B1_MAT0	17[2]	I/O	**PIO1_9 —** General purpose digital input/output pin.
		O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.

Table 3. LPC11C14 pin description table (LQFP48 package) *…continued*

Symbol	Pin	Type	Description
PIO1_10/AD6/ CT16B1_MAT1	30[4]	I/O	**PIO1_10 —** General purpose digital input/output pin.
		I	**AD6 —** A/D converter, input 6.
		O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	42[4]	I/O	**PIO1_11 —** General purpose digital input/output pin.
		I	**AD7 —** A/D converter, input 7.
PIO2_0 to PIO2_11		I/O	**Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/$\overline{DTR}$/SSEL1	2[2]	I/O	**PIO2_0 —** General purpose digital input/output pin.
		O	**$\overline{DTR}$ —** Data Terminal Ready output for UART.
		O	**SSEL1 —** Slave Select for SPI1.
PIO2_1/$\overline{DSR}$/SCK1	13[2]	I/O	**PIO2_1 —** General purpose digital input/output pin.
		I	**$\overline{DSR}$ —** Data Set Ready input for UART.
		I/O	**SCK1 —** Serial clock for SPI1.
PIO2_2/$\overline{DCD}$/MISO1	26[2]	I/O	**PIO2_2 —** General purpose digital input/output pin.
		I	**$\overline{DCD}$ —** Data Carrier Detect input for UART.
		I/O	**MISO1 —** Master In Slave Out for SPI1.
PIO2_3/$\overline{RI}$/MOSI1	38[2]	I/O	**PIO2_3 —** General purpose digital input/output pin.
		I	**$\overline{RI}$ —** Ring Indicator input for UART.
		I/O	**MOSI1 —** Master Out Slave In for SPI1.
CAN_RXD	19[5]	I	**CAN_RXD —** C_CAN receive data input.
CAN_TXD	20[5]	O	**CAN_TXD —** C_CAN transmit data output.
PIO2_6	1[2]	I/O	**PIO2_6 —** General purpose digital input/output pin.
PIO2_7	11[2]	I/O	**PIO2_7 —** General purpose digital input/output pin.
PIO2_8	12[2]	I/O	**PIO2_8 —** General purpose digital input/output pin.
PIO2_9	24[2]	I/O	**PIO2_9 —** General purpose digital input/output pin.
PIO2_10	25[2]	I/O	**PIO2_10 —** General purpose digital input/output pin.
PIO2_11/SCK0	31[2]	I/O	**PIO2_11 —** General purpose digital input/output pin.
		I/O	**SCK0 —** Serial clock for SPI0.
PIO3_0 to PIO3_5		I/O	**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_6 to PIO3_11 are not available.
PIO3_0/$\overline{DTR}$	36[2]	I/O	**PIO3_0 —** General purpose digital input/output pin.
		O	**$\overline{DTR}$ —** Data Terminal Ready output for UART.
PIO3_1/$\overline{DSR}$	37[2]	I/O	**PIO3_1 —** General purpose digital input/output pin.
		I	**$\overline{DSR}$ —** Data Set Ready input for UART.
PIO3_2/$\overline{DCD}$	43[2]	I/O	**PIO3_2 —** General purpose digital input/output pin.
		I	**$\overline{DCD}$ —** Data Carrier Detect input for UART.
PIO3_3/$\overline{RI}$	48[2]	I/O	**PIO3_3 —** General purpose digital input/output pin.
		I	**$\overline{RI}$ —** Ring Indicator input for UART.
PIO3_4	18[2]	I/O	**PIO3_4 —** General purpose digital input/output pin.

Table 3. LPC11C14 pin description table (LQFP48 package) *…continued*

Symbol	Pin	Type	Description
PIO3_5	21[2]	I/O	**PIO3_5 —** General purpose digital input/output pin.
V_{DD}	8;44	I	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6[6]	I	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[6]	O	Output from the oscillator amplifier.
V_{SS}	5; 41	I	Ground.

[1] See Figure 25 for reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 24).

[3] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 24).

[5] 5 V tolerant digital I/O pad without pull-up/pull-down resistors.

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC11C12/C14 contain 32 kB (LPC11C14) or 16 kB (LPC11C12) of on-chip flash memory.

7.3 On-chip SRAM

The LPC11C12/C14 contain a total of 8 kB on-chip static RAM memory.

7.4 Memory map

The LPC11C12/C14 incorporates several distinct memory regions, shown in the following figures. Figure 3 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

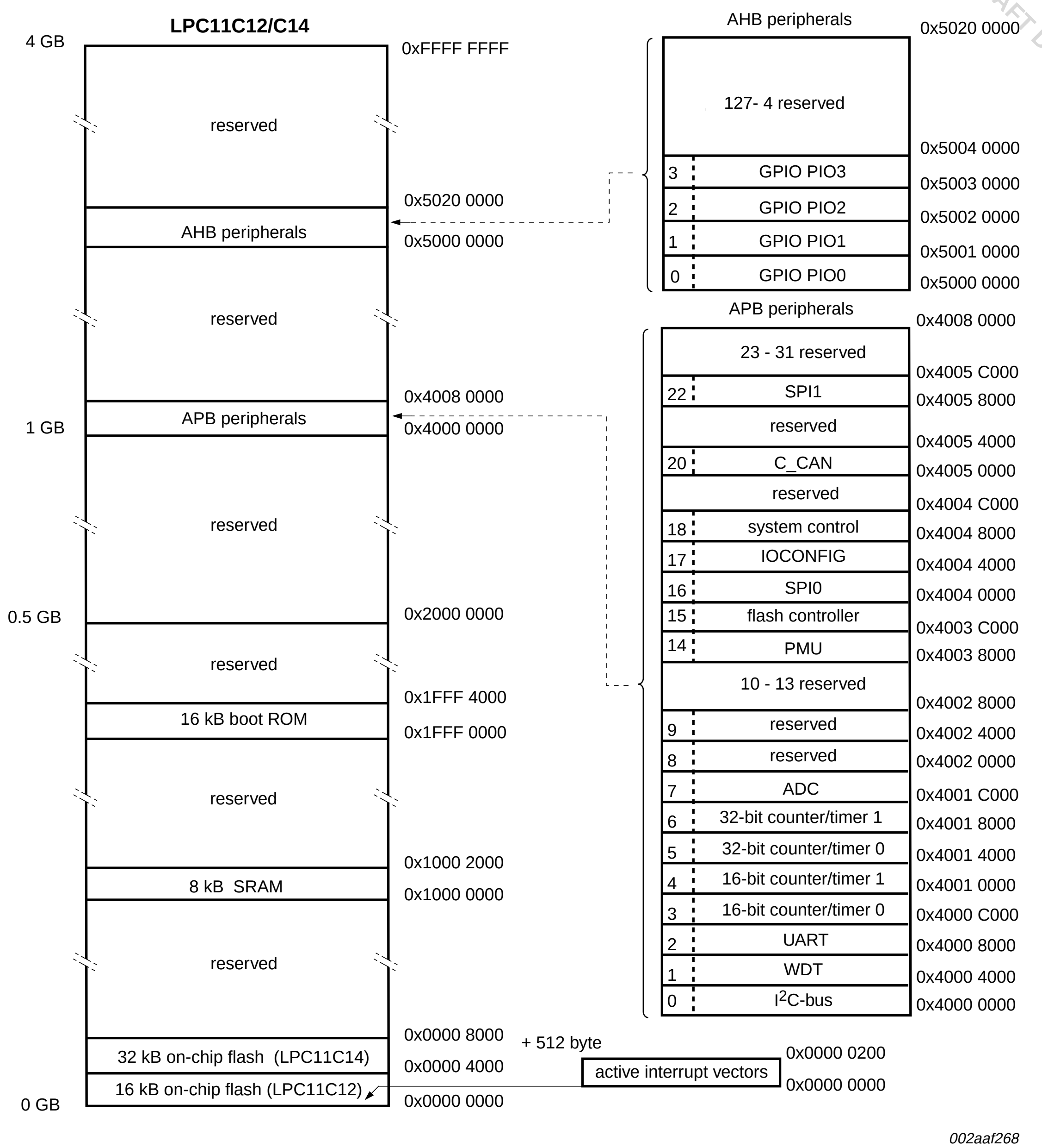


Fig 3. LPC11C12/C14 memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11C12/C14, the NVIC supports 32 vectored interrupts including 13 inputs to the start logic from individual GPIO pins.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of 40 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11C12/C14 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of 40 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All GPIO pins default to inputs with pull-ups enabled after reset except for the I^2C-bus true open-drain pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin (except PIO0_4 and PIO0_5).

7.8 UART

The LPC11C12/C14 contain one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.9 SPI serial I/O controller

The LPC11C12/C14 contain two SPI controllers. Both SPI controllers support SSP features.

The SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 I^{2}C-bus serial I/O controller

The LPC11C12/C14 contain one I^{2}C-bus controller.

The I^{2}C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or

receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I²C-interface is a standard I²C-bus compliant interface with open-drain pins. The I²C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 C_CAN controller

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a very high level of security.

On-chip C_CAN drivers provide an API for initialization and communication using CAN and CANopen standards.

7.11.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.
- The C_CAN API includes the following functions:
  - C_CAN set-up and initialization
  - C_CAN send and receive messages

- C_CAN status
- CANopen object dictionary
- CANopen SDO expedited communication
- CANopen SDO segmented communication primitives
- CANopen SDO fall-back handler
- Flash ISP programming via C_CAN supported.

7.12 10-bit ADC

The LPC11C12/C14 contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.12.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.13 General purpose external event counter/timers

The LPC11C12/C14 includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.13.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.

– Do nothing on match.

7.14 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a selectable time period.

7.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the Watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.16 Clocking and power control

7.16.1 Crystal oscillators

The LPC11C12/C14 include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11C12/C14 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the LPC11C12/C14 clock generation.

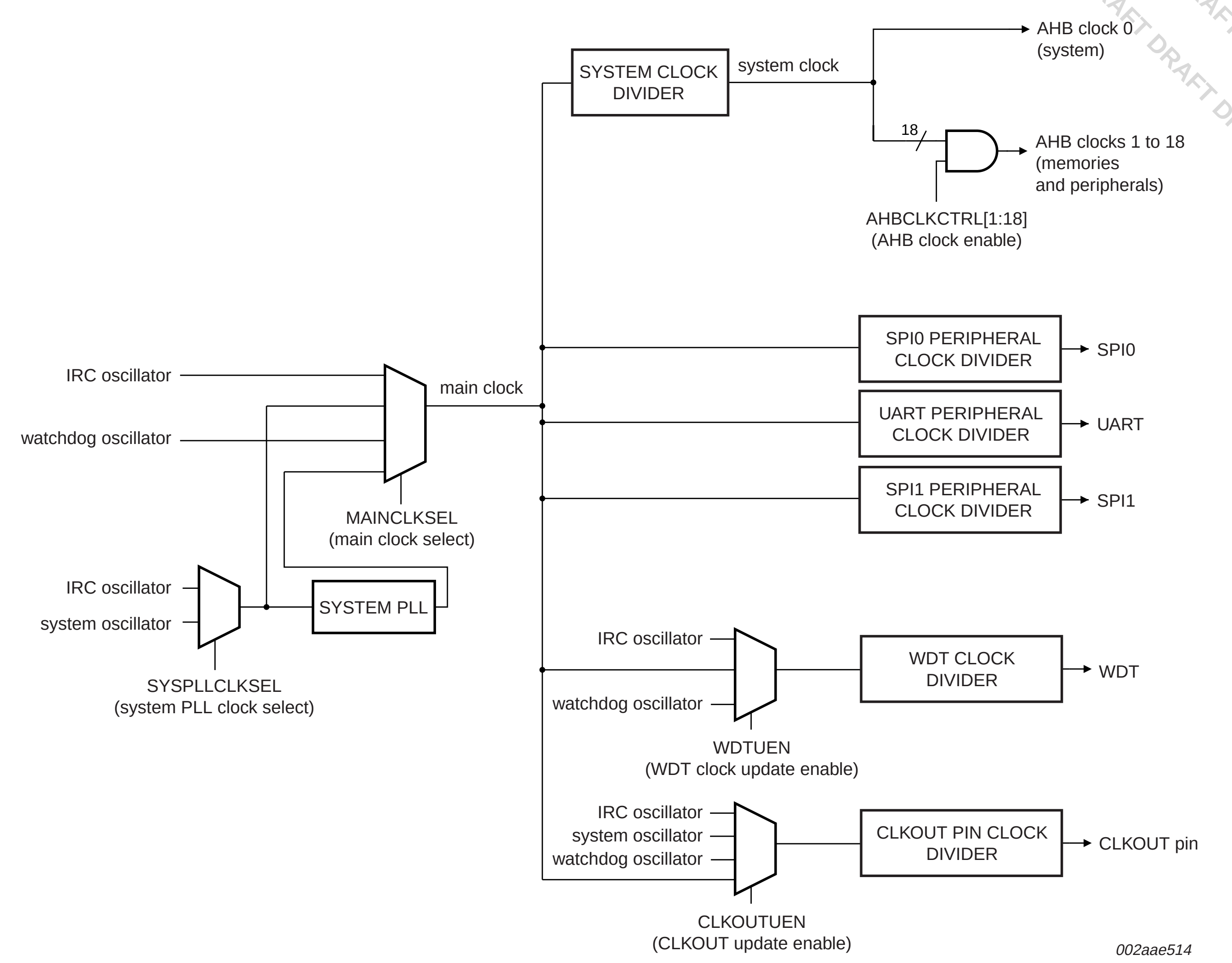


Fig 4. LPC11C12/C14 clock generation block diagram

7.16.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC11C12/C14 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.16.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.16.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 % (see Table 11).

7.16.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.16.3 Clock output

The LPC11C12/C14 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.16.4 Wake-up process

The LPC11C12/C14 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the system oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.16.5 Power control

The LPC11C12/C14 support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.16.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.16.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition analog blocks can be shut down for increased power savings. The user can configure the Deep-sleep mode to a large extent, selecting any of the oscillators, the PLL, BOD, the ADC, and the flash to be shut down or remain powered during Deep-sleep mode. The user can also select which of the oscillators and analog blocks will be powered up after the chip exits from Deep-sleep mode.

The GPIO pins (13 pins total) serve as external wake-up pins to a dedicated start logic to wake up the chip from Deep-sleep mode.

The timing of the wake-up process from Deep-sleep mode depends on which blocks are selected to be powered down during deep-sleep.

For lowest power consumption, the clock source should be switched to IRC before entering Deep-sleep mode, all oscillators and the PLL should be turned off during deep-sleep, and the IRC should be selected as clock source when the chip wakes up from deep-sleep. The IRC can be switched on and off glitch-free and provides a clean clock signal after start-up.

If power consumption is not a concern, any of the oscillators and/or the PLL can be left running in Deep-sleep mode to obtain short wake-up times when waking up from deep-sleep.

7.16.5.3 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC11C12/C14 can wake up from Deep power-down mode via the WAKEUP pin.

7.17 System control

7.17.1 Reset

Reset has four sources on the LPC11C12/C14: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.17.2 Brownout detection

The LPC11C12/C14 includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

7.17.3 Code security (Code Read Protection - CRP)

This feature of the LPC11C12/C14 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC11Cx user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the *LPC11Cx user manual*.

7.17.4 Boot loader

The boot loader controls initial operation after reset and also provides the means to program the flash memory. This could be initial programming of a blank device, erasure and re-programming of a previously programmed device, or programming of the flash memory by the application program in a running system.

The boot loader code is executed every time the part is reset or powered up. The loader can either execute the user application code or the ISP command handler via UART or C_CAN. A LOW level during reset applied to the PIO0_1 pin is considered as an external hardware request to start the ISP command handler. The state of PIO0_3 at reset determines whether the UART (PIO0_3 HIGH) or the C_CAN (PIO0_3 LOW) interface will be used.

The C_CAN ISP command handler uses the CANopen protocol and data organization method. C_CAN ISP commands have the same functionality as UART ISP commands.

7.17.5 APB interface

The APB peripherals are located on one APB bus.

7.17.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.17.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.17.8 Memory mapping control

The Cortex-M0 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M0 address space. The vector table must be located on a 128 word (512 byte) boundary.

7.18 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	–0.5	+5.5	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	–5000	+5000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Static characteristics

Table 5. Static characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4] [5][6][7]	-	3	-	mA
		system clock = 50 MHz V_{DD} = 3.3 V	[2][3][6] [5][7][8]	-	9	-	mA
		Sleep mode; system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4] [5][6][7]	-	2	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V	[2][3][5] [9]	-	6	-	µA
		Deep power-down mode; V_{DD} = 3.3 V	[2][10]	-	220	-	nA
Standard port pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[11][12] [13]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = –4 mA	[14]	V_{DD} – 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OH} = –3 mA	[14]	V_{DD} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	[14]	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA	[14]	-	-	0.4	V

Table 5. Static characteristics *...continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; $2.0\ V \leq V_{DD} \leq 3.6\ V$	[14]	–4	-	-	mA
		$1.8\ V \leq V_{DD} < 2.0\ V$	[14]	–3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $2.0\ V \leq V_{DD} \leq 3.6\ V$	[14]	4	-	-	mA
		$1.8\ V \leq V_{DD} < 2.0\ V$	[14]	3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	–45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; $2.0\ V \leq V_{DD} \leq 3.6\ V$		–15	–50	–85	µA
		$1.8\ V \leq V_{DD} < 2.0\ V$		–10	–50	–85	µA
		$V_{DD} < V_I < 5$ V		0	0	0	µA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[11][12][13]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.0\ V \leq V_{DD} \leq 3.6$ V; I_{OH} = –4 mA	[14]	$V_{DD} - 0.4$	-	-	V
		$1.8\ V \leq V_{DD} < 2.0$ V; I_{OH} = –3 mA	[14]	$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.0\ V \leq V_{DD} \leq 3.6$ V; I_{OL} = 4 mA	[14]	-	-	0.4	V
		$1.8\ V \leq V_{DD} < 2.0$ V; I_{OL} = 3 mA	[14]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; $V_{DD} \geq 2.5$ V	[14]	20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $2.0\ V \leq V_{DD} \leq 3.6\ V$	[14]	4	-	-	mA
		$1.8\ V \leq V_{DD} < 2.0\ V$	[14]	3	-	-	mA

Table 5. Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	–45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		–15	–50	–85	µA
		2.0 V ≤ V_{DD} ≤ 3.6 V					
		1.8 V ≤ V_{DD} < 2.0 V		–10	–50	–85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I²C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.5V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as standard mode pins	[14]	4	-	-	mA
		2.0 V ≤ V_{DD} ≤ 3.6 V					
		1.8 V ≤ V_{DD} < 2.0 V	[14]	3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as Fast-mode Plus pins	[14]	20	-	-	mA
		2.0 V ≤ V_{DD} ≤ 3.6 V					
		1.8 V ≤ V_{DD} < 2.0 V	[14]	16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[16]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			–0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			–0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] Pin CAN_RXD pulled LOW externally.

[6] BOD disabled.

[7] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0xFFFF FDFF.

[10] WAKEUP pin pulled HIGH externally.

[11] Including voltage on outputs in 3-state mode.

[12] V_{DD} supply voltage must be present.

[13] 3-state outputs go into 3-state mode in Deep power-down mode.

[14] Accounts for 100 mV voltage drop in all supply lines.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To V_{SS}.

Table 6. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

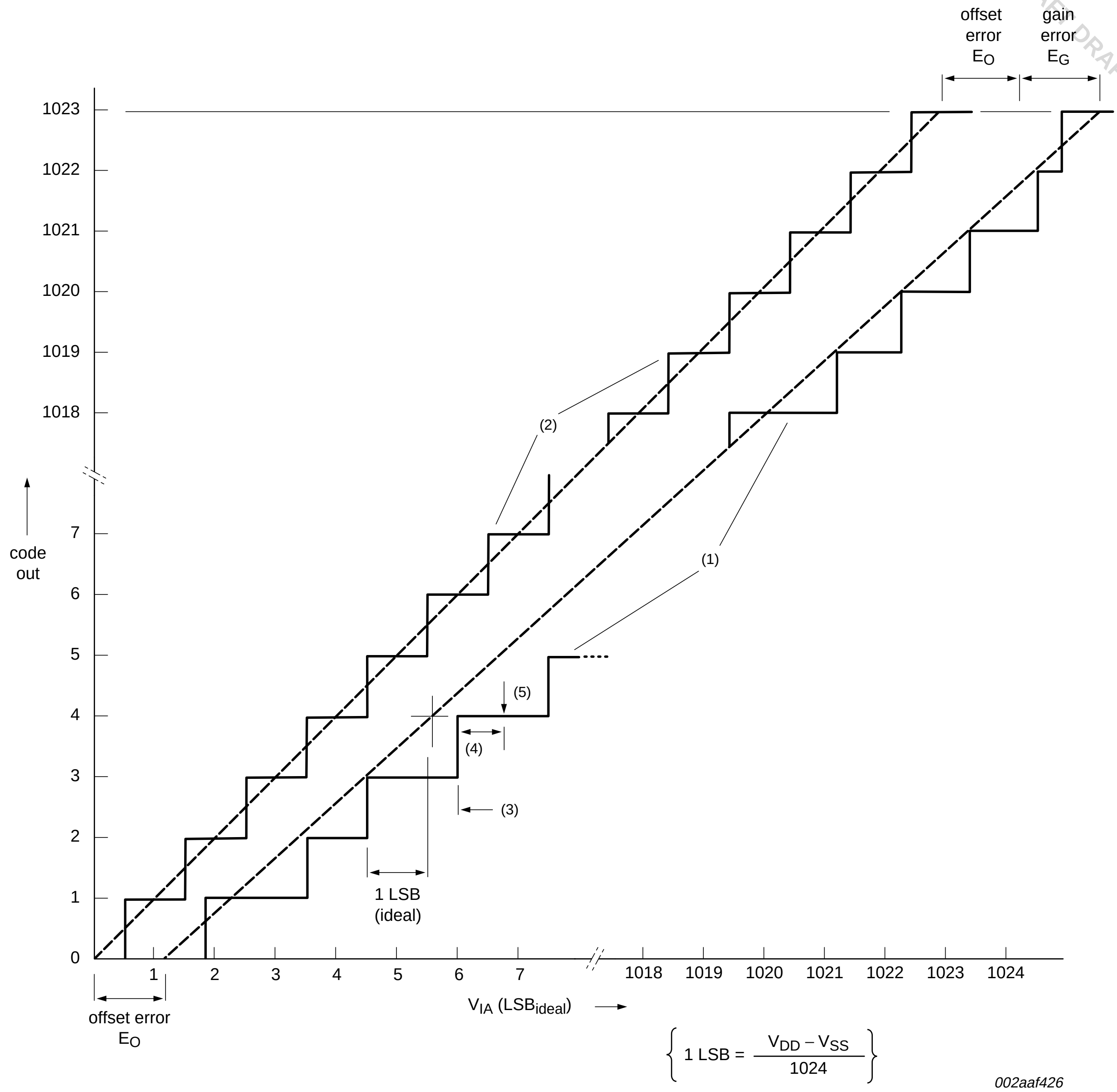
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 4.5 MHz and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential linearity error (E_D).
(4) Integral non-linearity ($E_{L(adj)}$).
(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics

9.1 BOD static characteristics

Table 7. BOD static characteristics[1]

T_{amb} = 25 °C.

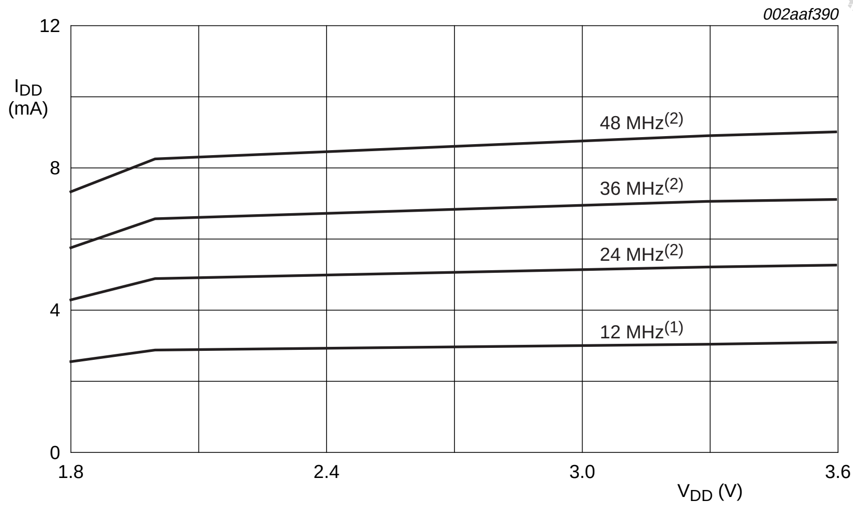
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC11Cx user manual*.

9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC11Cx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

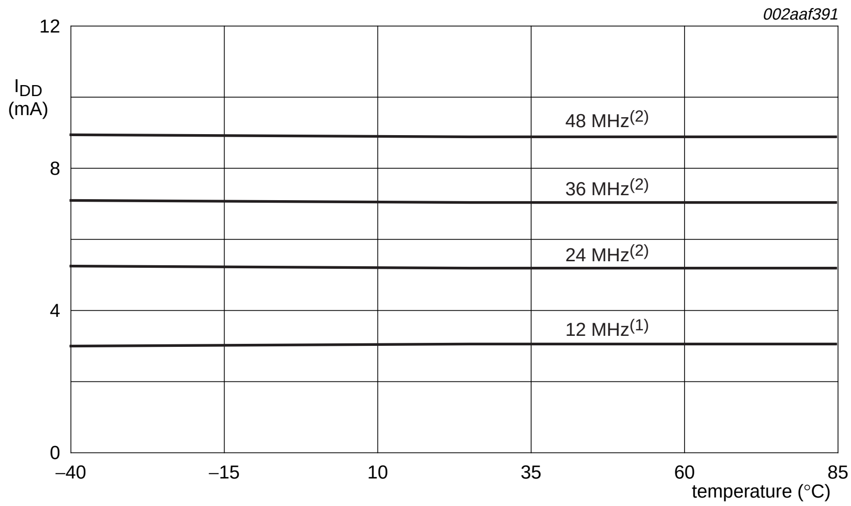


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the AHBCLKCTRL register (AHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; pin CAN_RXD pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 6. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies

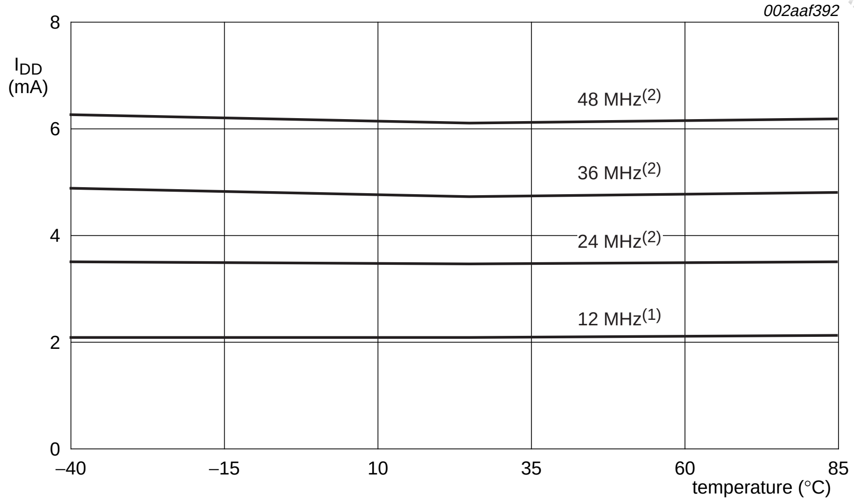


Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the AHBCLKCTRL register (AHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; pin CAN_RXD pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 7. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

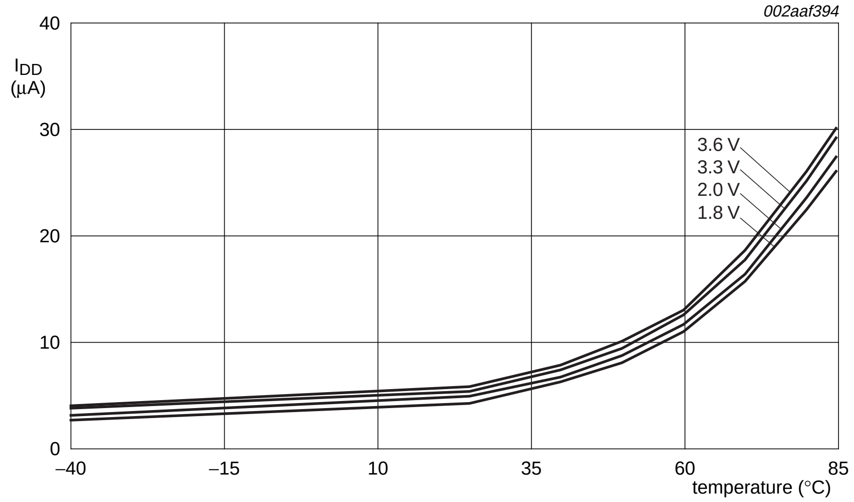


Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the AHBCLKCTRL register (AHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; pin CAN_RXD pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 8. Sleep mode: Typical supply current I_{DD}versus temperature for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0xFFFF FDFF); pin CAN_RXD pulled LOW externally.

Fig 9. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

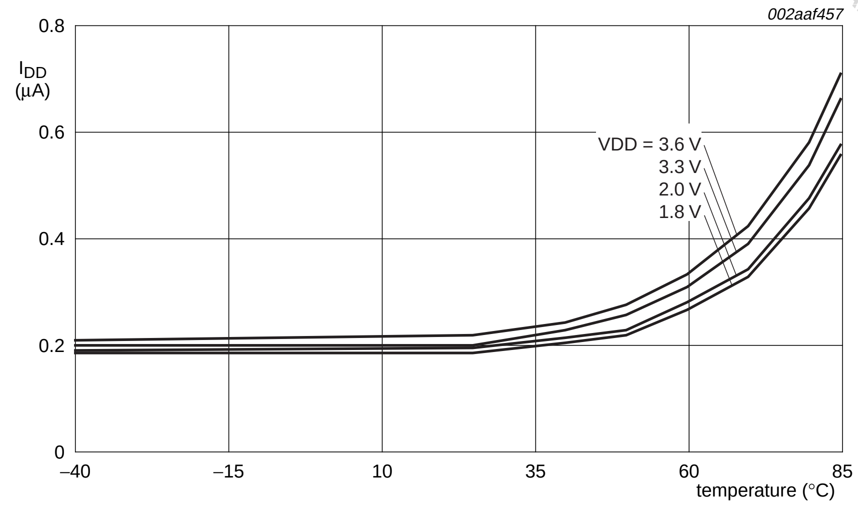
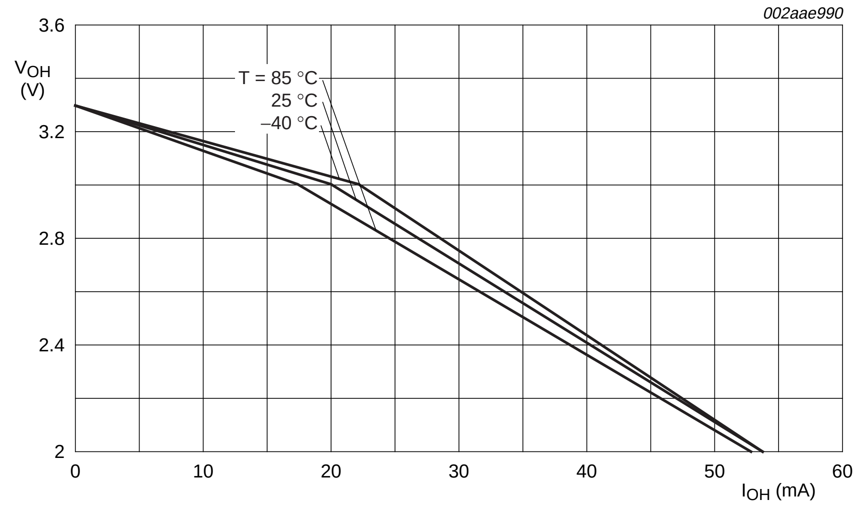


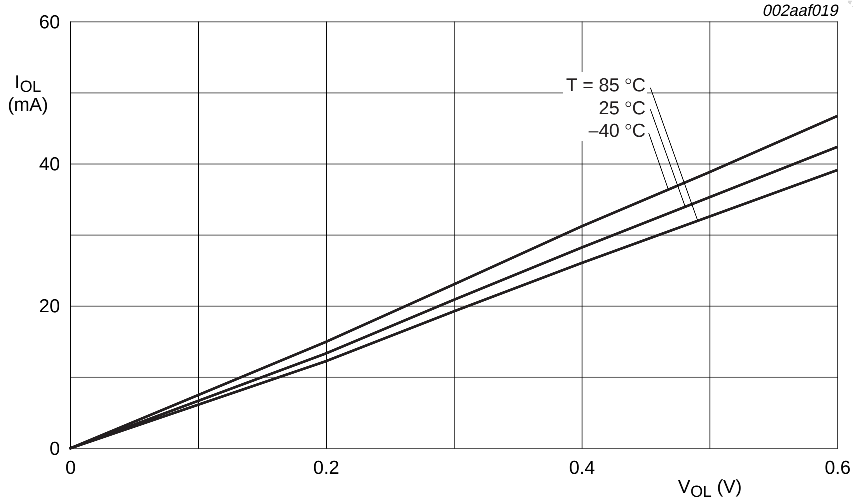
Fig 10. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

9.3 Electrical pin characteristics



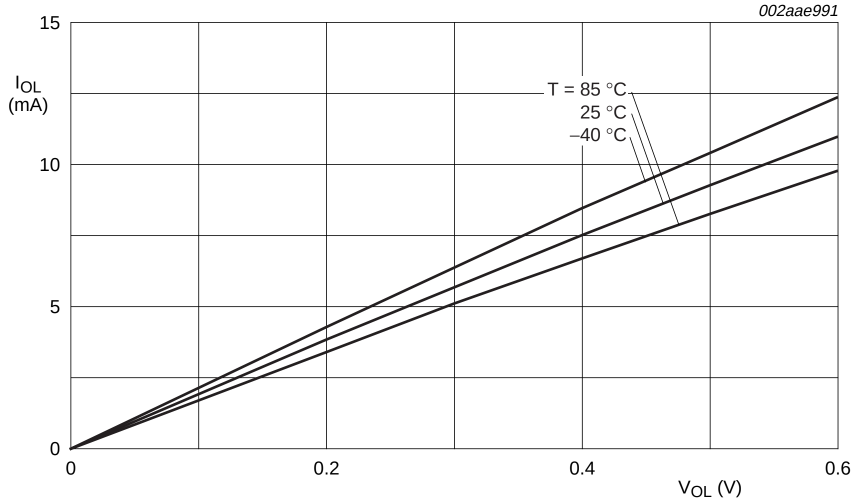
Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 11. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



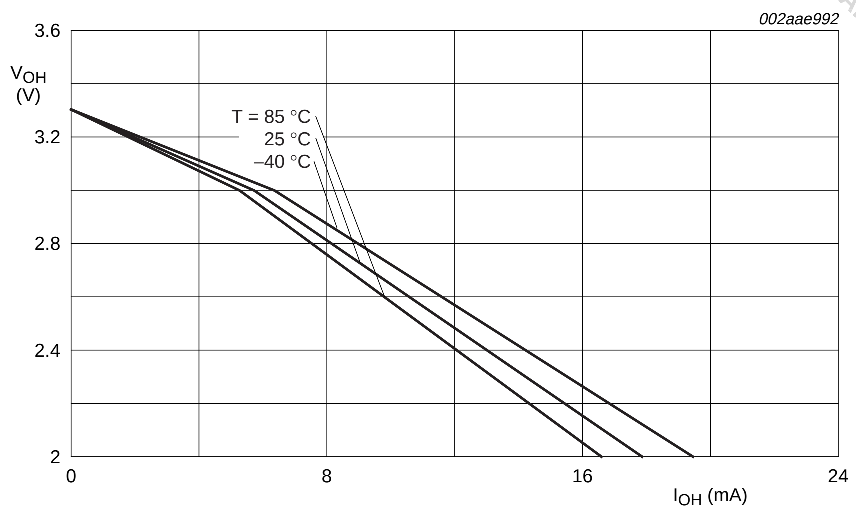
Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 12. I²C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



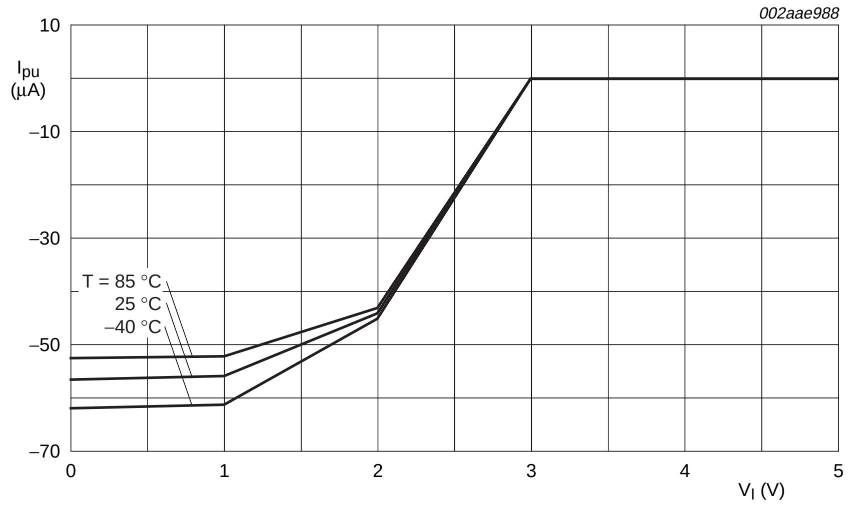
Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 13. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



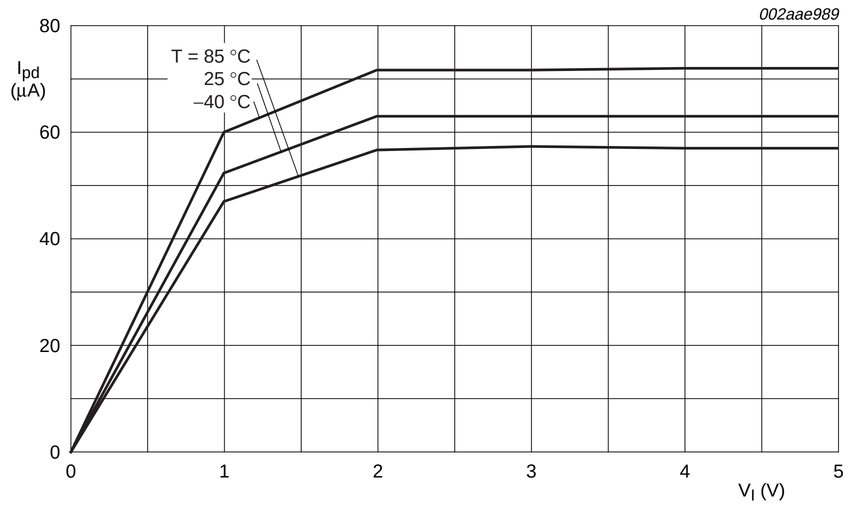
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 14. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 15. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 16. Typical pull-down current I_{pd} versus input voltage V_I

10. Dynamic characteristics

10.1 Flash memory

Table 8. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

10.2 External clock

Table 9. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

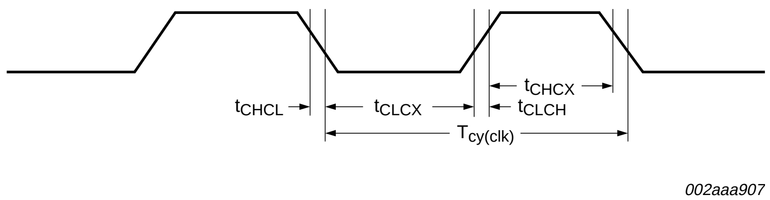


Fig 17. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

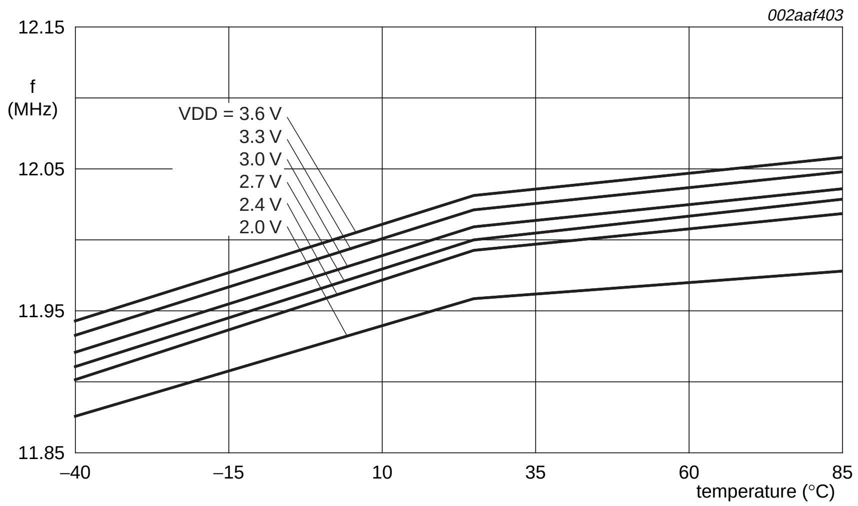
10.3 Internal oscillators

Table 10. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 18. Internal RC oscillator frequency vs. temperature

Table 11. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{osc}	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the LPC11Cx user manual.

10.4 I/O pins

Table 12. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 I^{2}C-bus

Table 13. Dynamic characteristic: I^{2}C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I^{2}C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

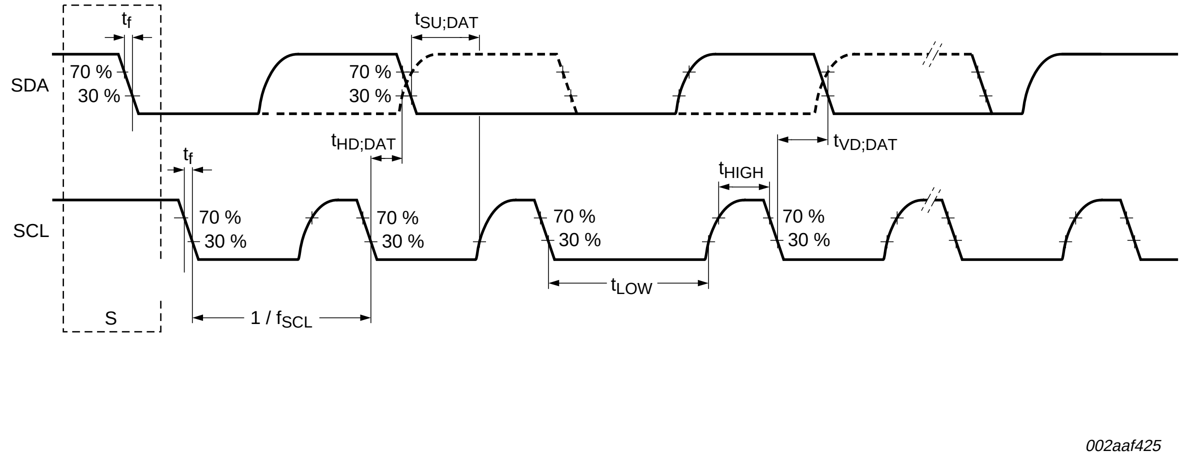


Fig 19. I^{2}C-bus pins clock timing

10.6 SPI interfaces

Table 14. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
$T_{cy(clk)}$	clock cycle time		[1]	40	-	-	ns
SPI master (in SPI mode)							
t_{DS}	data set-up time	in SPI mode $2.0\ V \leq V_{DD} \leq 3.6\ V$	[2]	27	-	-	ns
		$1.8\ V \leq V_{DD} < 2.0\ V$		36	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns

Table 14. Dynamic characteristics of SPI pins in SPI mode

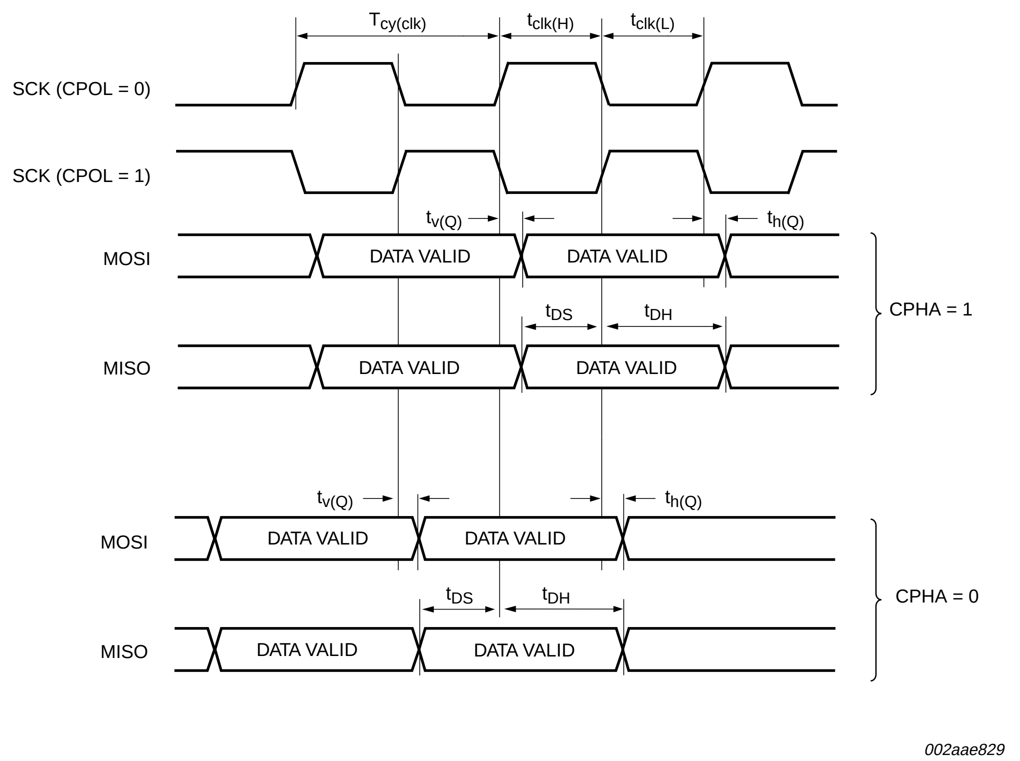
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

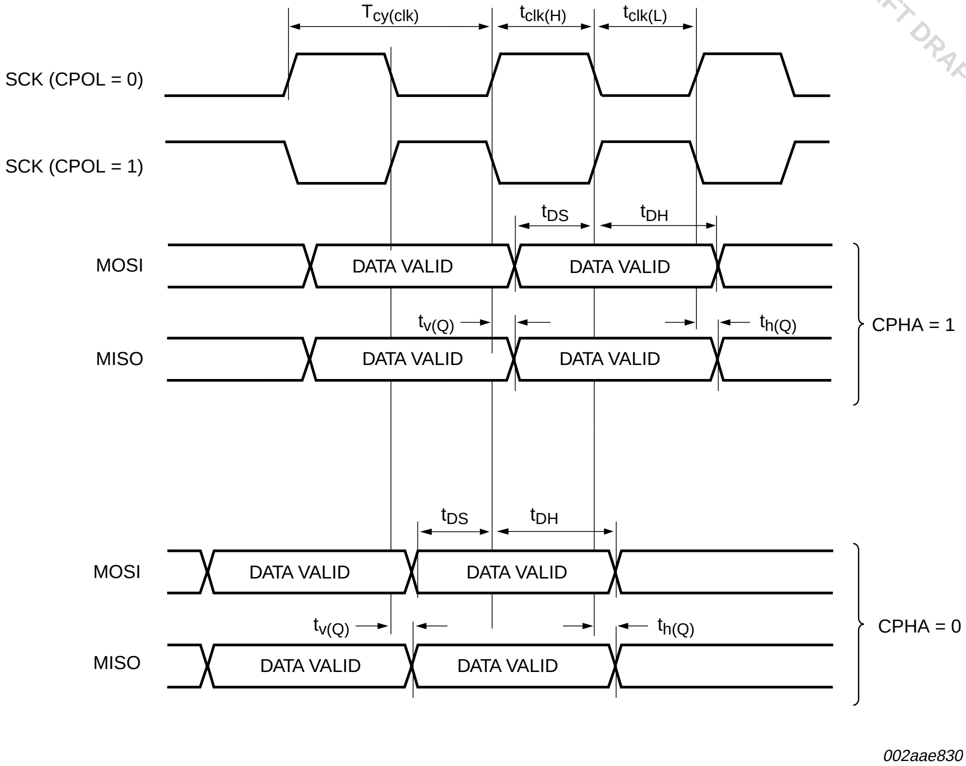
[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: V_{DD} = 3.3 V.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 20. SPI master timing in SPI mode



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 21. SPI slave timing in SPI mode

11. Application information

11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC11C12/C14 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

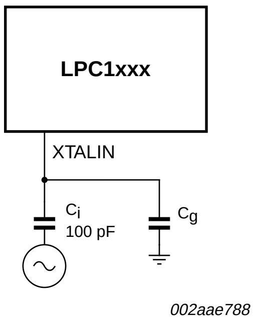


Fig 22. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 22), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 23 and in Table 15 and Table 16. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 23 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 15).

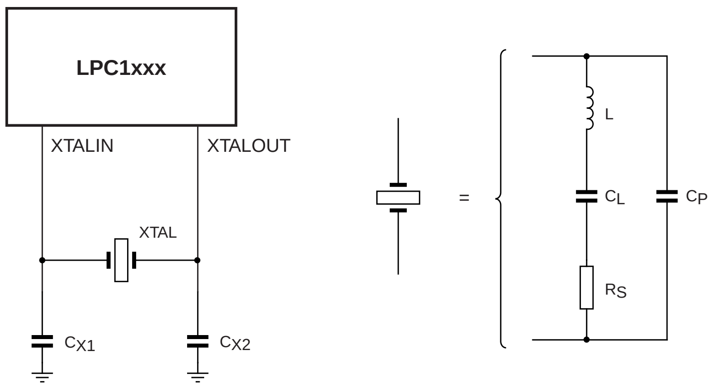


Fig 23. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 15. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 16. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

11.3 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

11.4 Standard I/O pad configuration

Figure 24 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

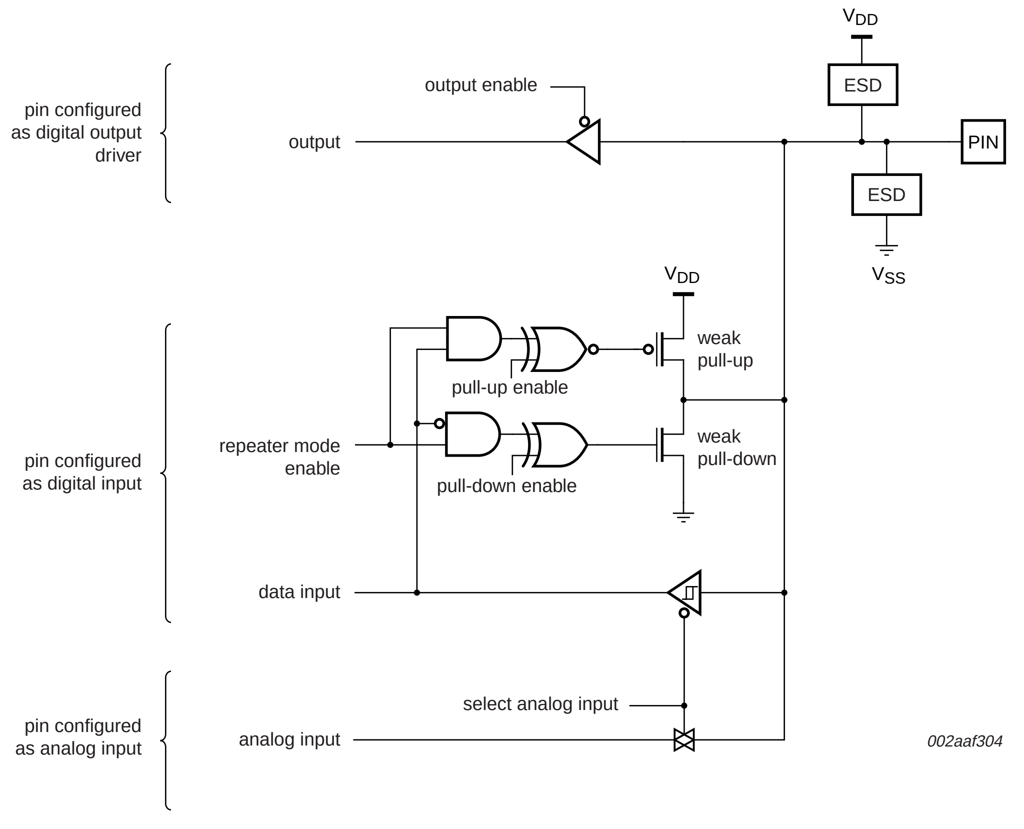


Fig 24. Standard I/O pad configuration

11.5 Reset pad configuration

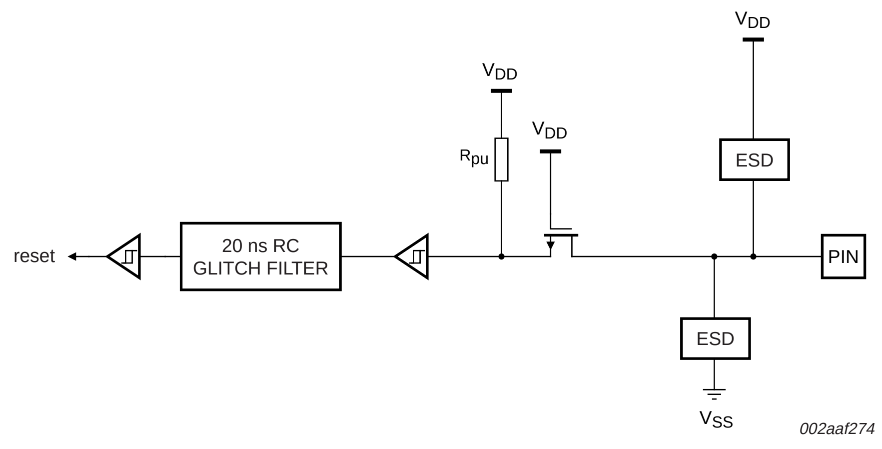
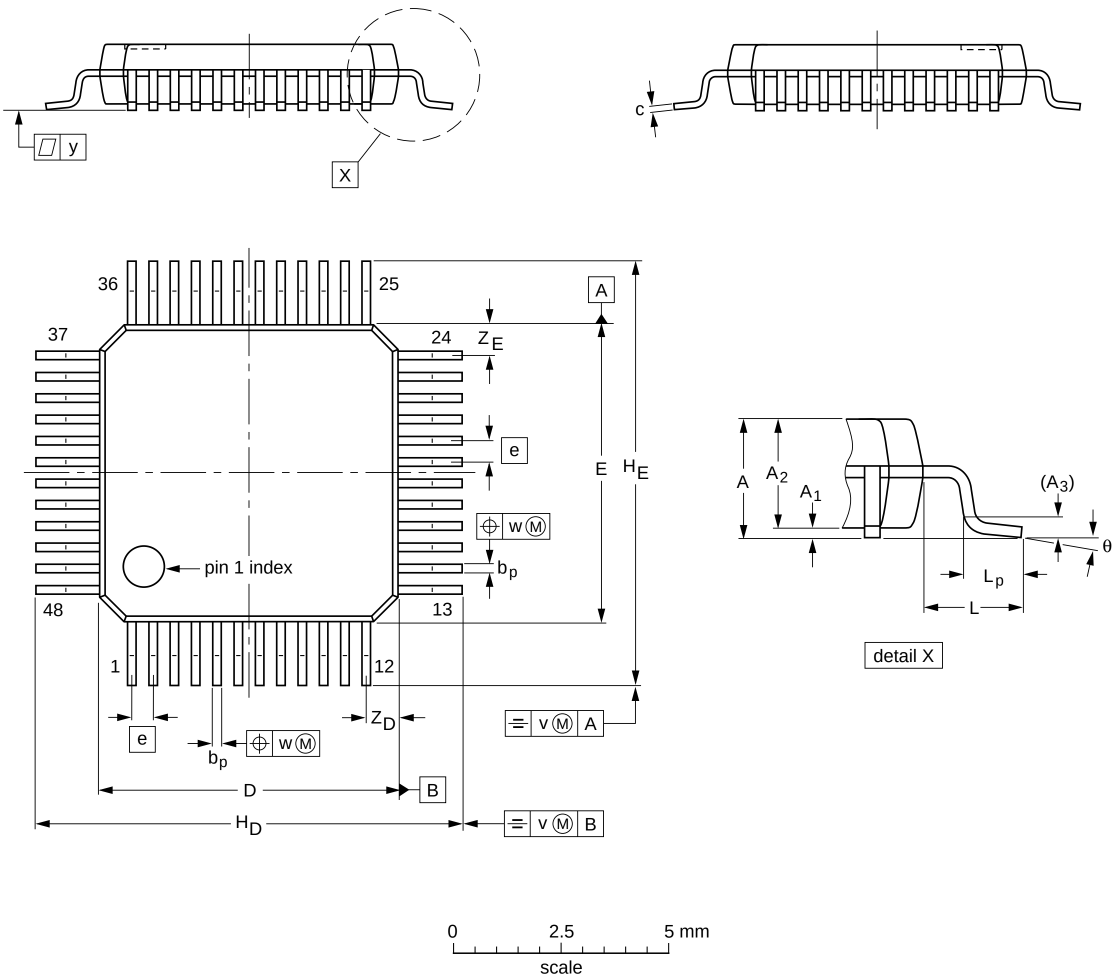


Fig 25. Reset pad configuration

12. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 26. Package outline SOT313-2 (LQFP48)

13. Abbreviations

Table 17. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
CAN	Controller Area Network
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SDO	Service Data Object
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

14. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11C12_C14_0.05	<tbd>	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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