

TIBPAL16L8-25C, TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16L8-30M, TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE IMPACT™ PAL® CIRCUITS

SRPS059A – FEBRUARY 1984 – REVISED DECEMBER 2010

- **High-Performance Operation:**
Propagation Delay
C Suffix . . . 25 ns Max
M Suffix . . . 30 ns Max
- **Functionally Equivalent, but Faster Than**
PAL16L8A, PAL16R4A, PAL16R6A, and
PAL16R8A
- **Power-Up Clear on Registered Devices (All**
Register Outputs Are Set High, but Voltage
Levels at the Output Pins Go Low)
- **Package Options Include Both Plastic and**
Ceramic Chip Carriers in Addition to Plastic
and Ceramic DIPs
- **Dependable Texas Instruments Quality and**
Reliability

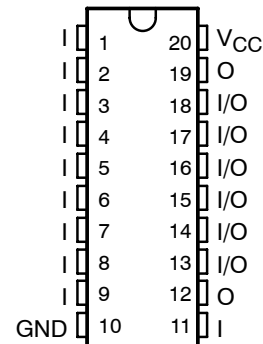
DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

description

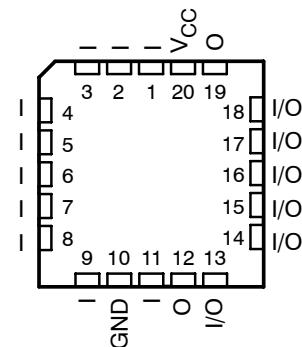
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



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PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



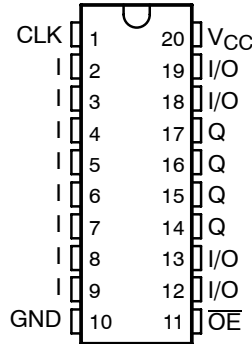
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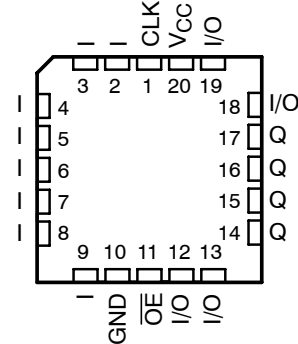
TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

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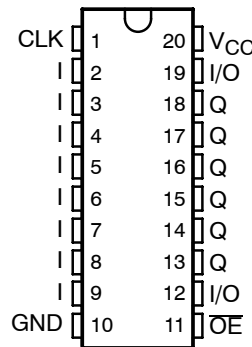
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M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



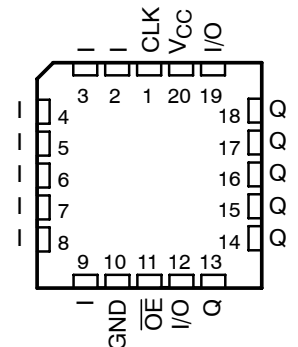
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M SUFFIX . . . FK PACKAGE
(TOP VIEW)



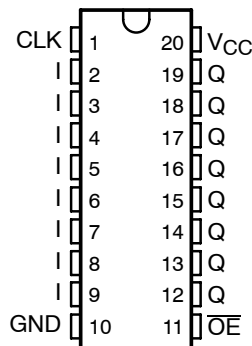
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C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



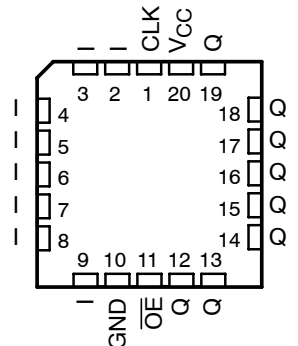
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)

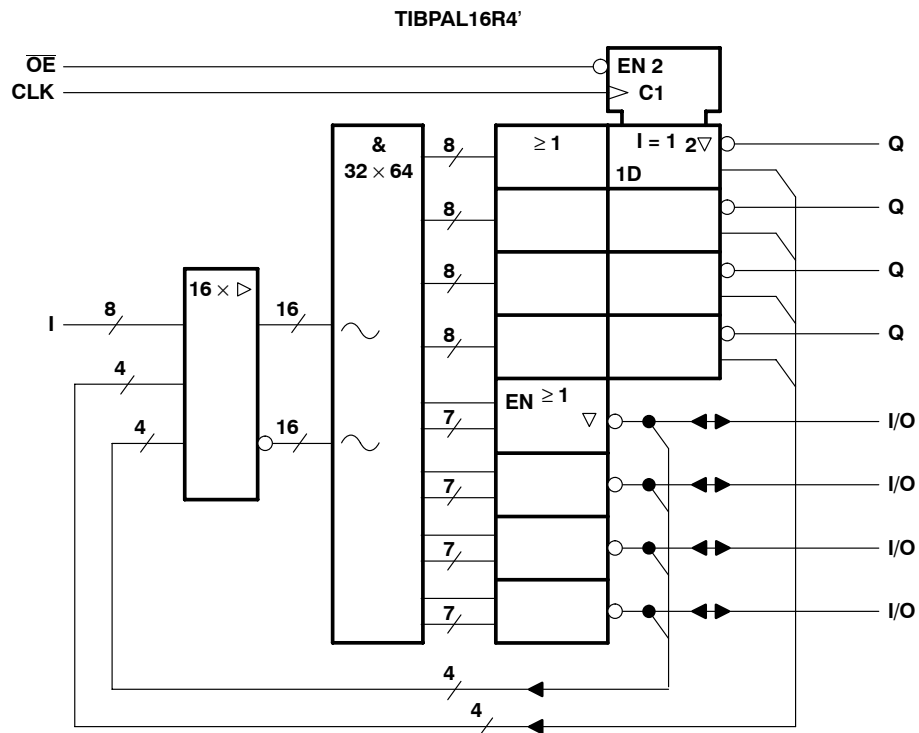
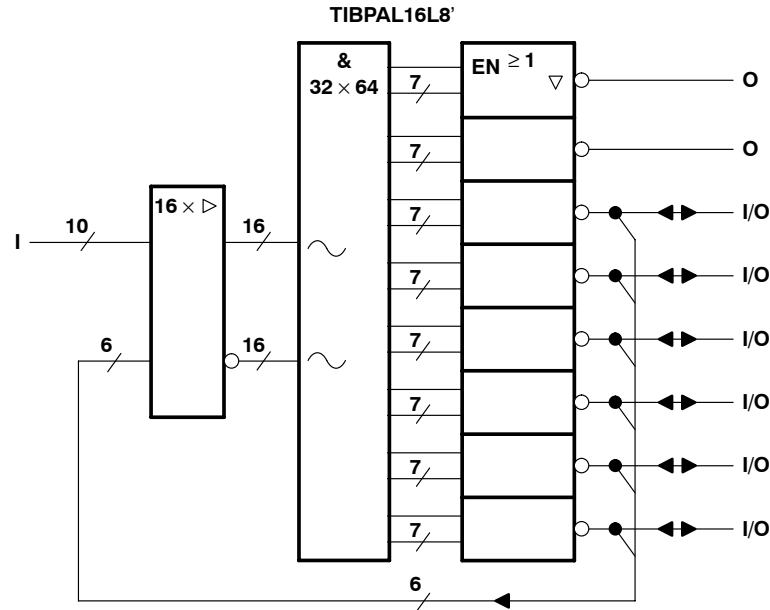


TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
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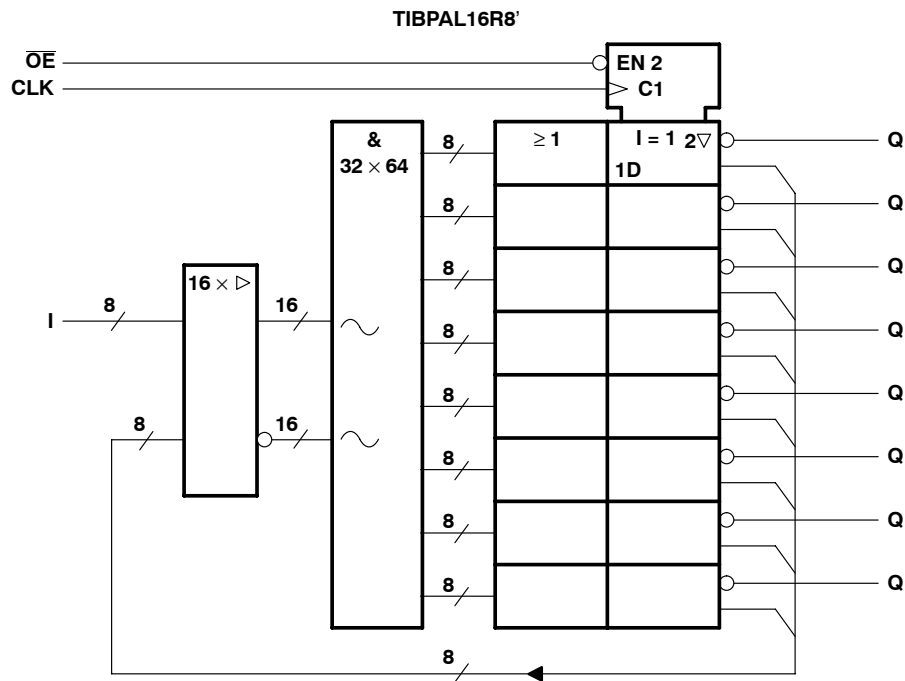
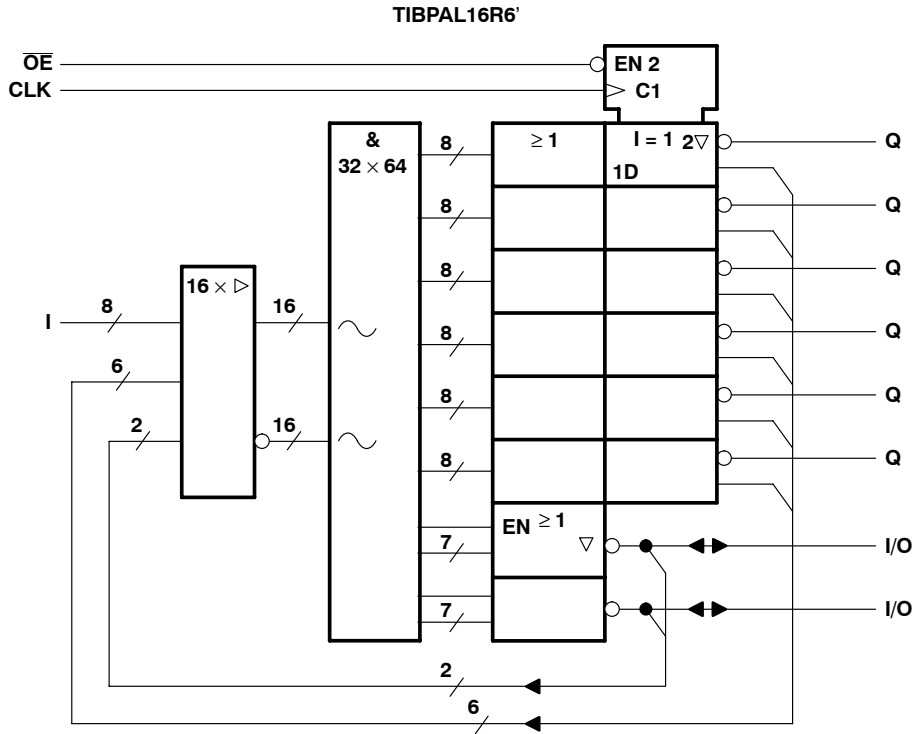
functional block diagrams (positive logic)



~ denotes fused inputs

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
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functional block diagrams (positive logic)

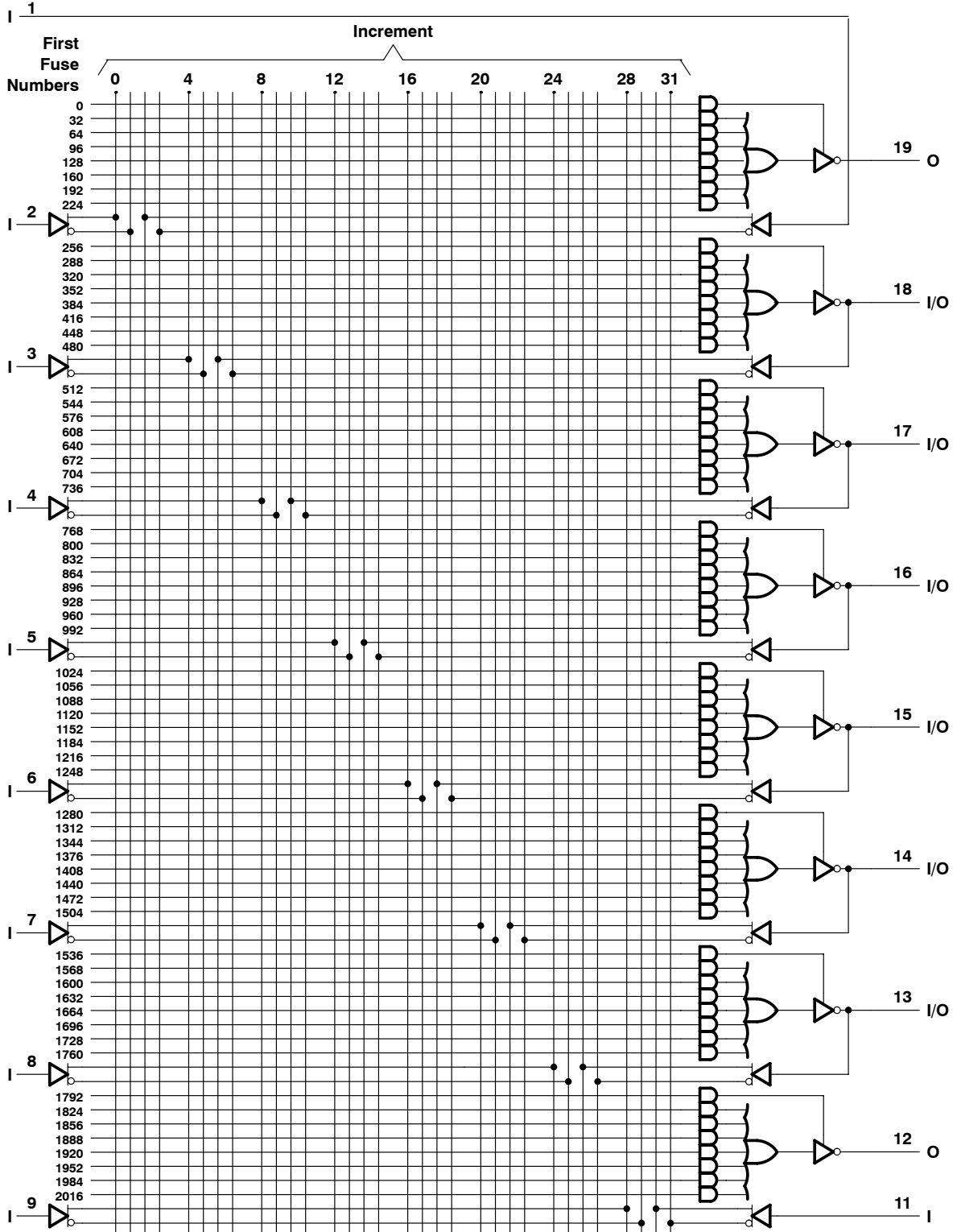


⋈ denotes fused inputs

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

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logic diagram (positive logic)

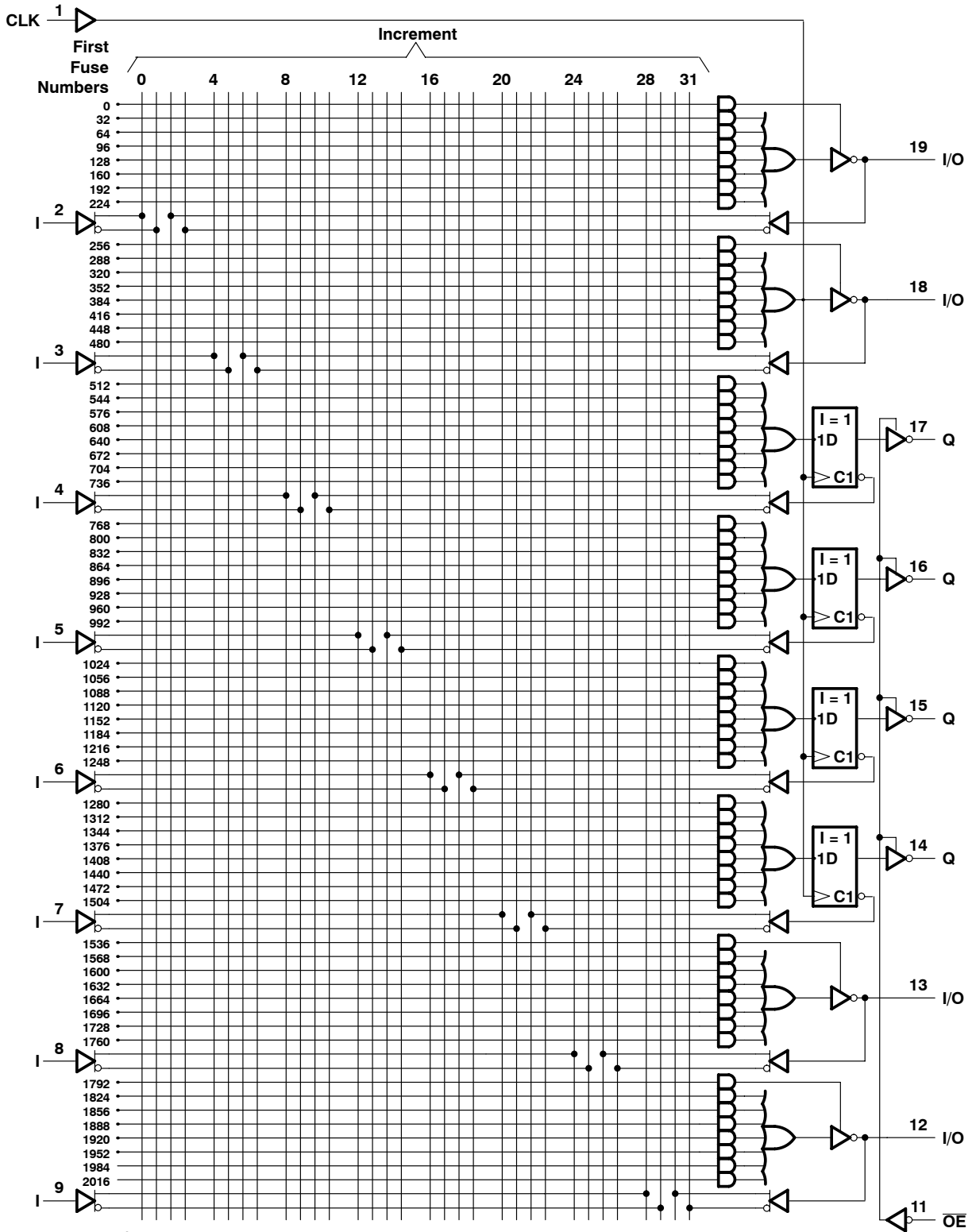


Fuse number = First fuse number + Increment

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

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logic diagram (positive logic)

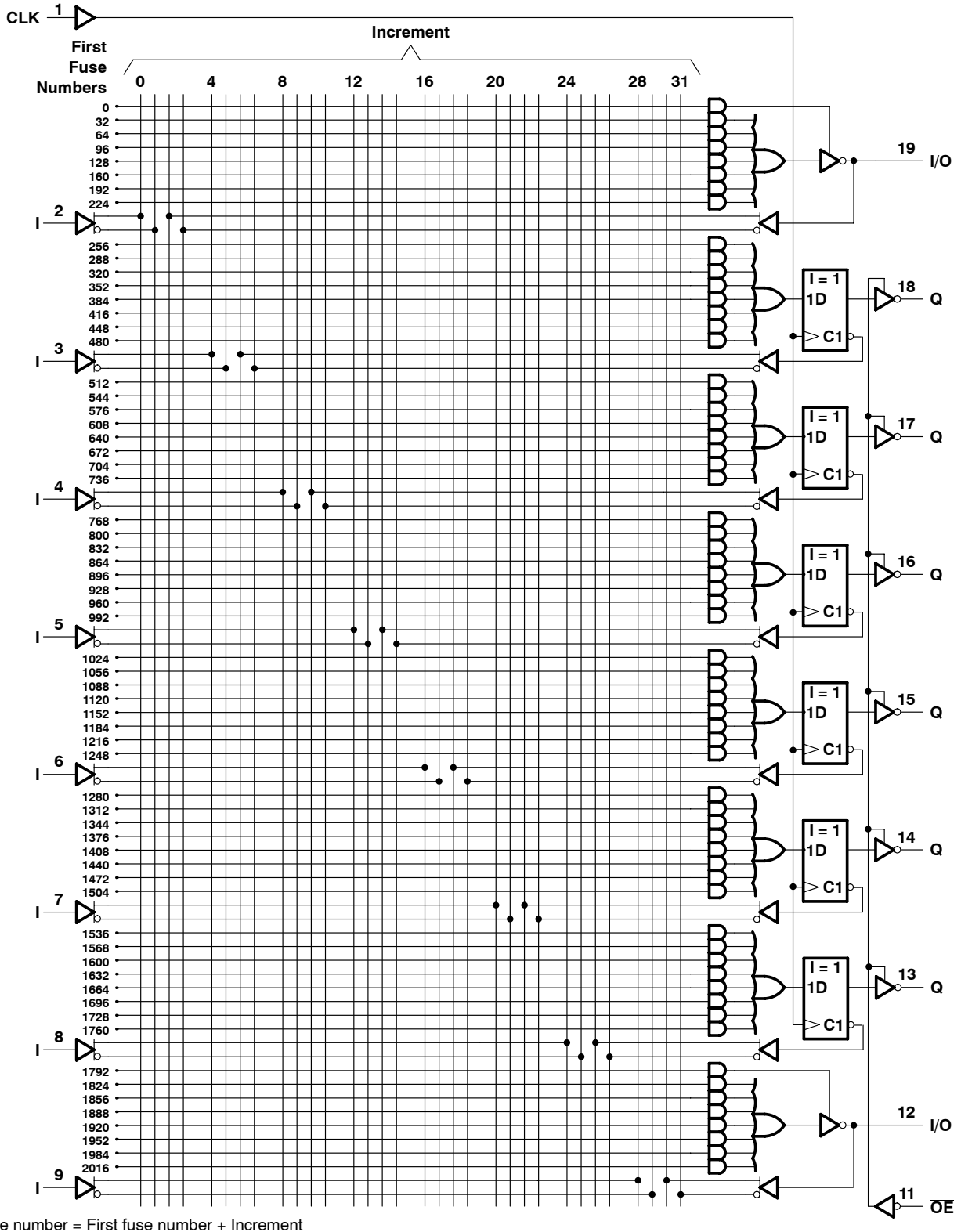


Fuse number = First fuse number + Increment

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

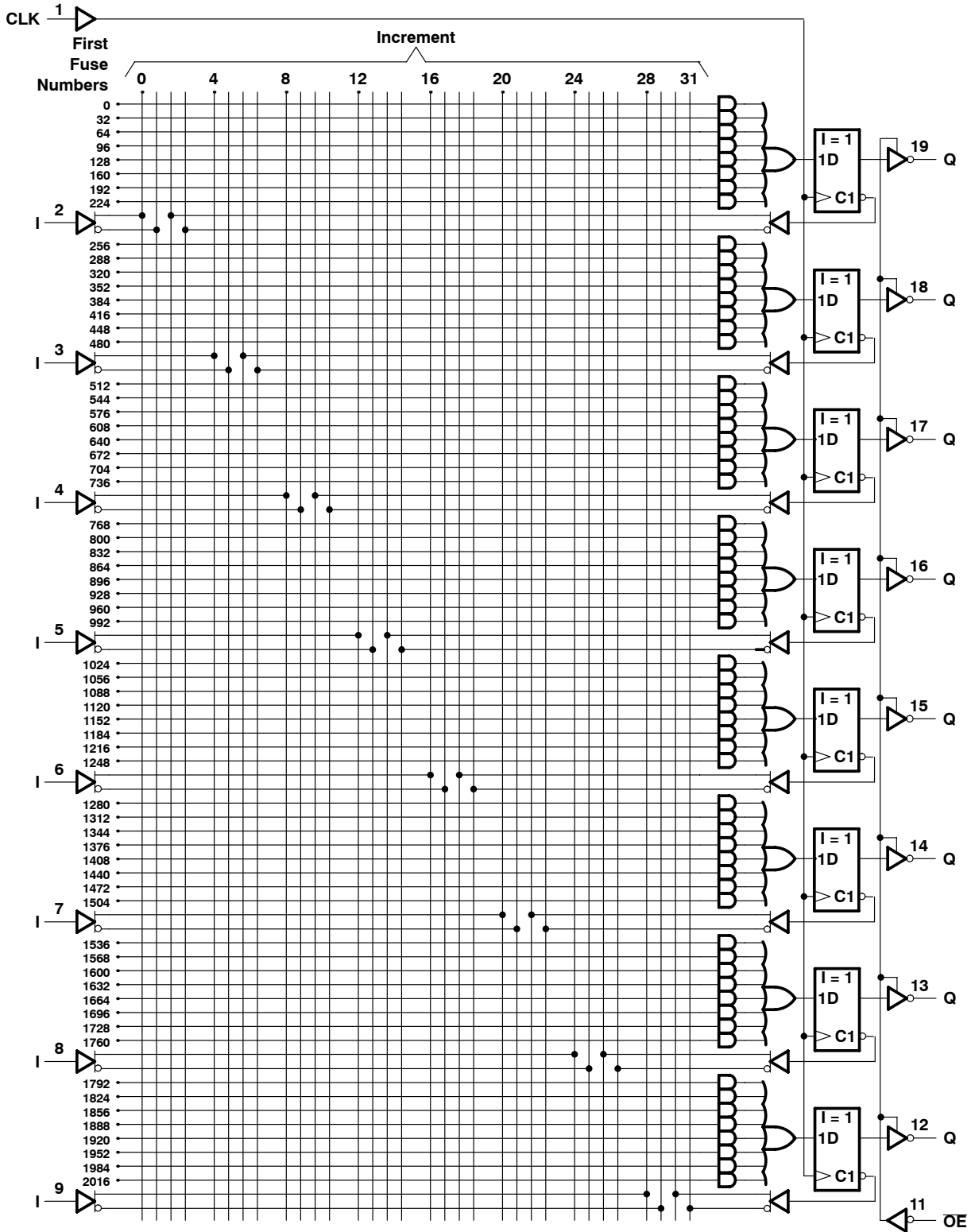
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logic diagram (positive logic)



TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS
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logic diagram (positive logic)



Fuse number = First fuse number + Increment

**TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range, T_{stg}	-65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-3.2	mA
I_{OL}	Low-level output current			24	mA
f_{clock}	Clock frequency	0		30	MHz
t_w	Pulse duration, clock (see Note 2)	High	10		ns
		Low	15		
t_{su}	Setup time, input or feedback before clock↑	20			ns
t_h	Hold time, input or feedback after clock↑	0			ns
T_A	Operating free-air temperature	0	25	75	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.75 V,	I _I = -18 mA			-1.5	V
V _{OH}	V _{CC} = 4.75 V,	I _{OH} = -3.2 mA	2.4	3.3		V
V _{OL}	V _{CC} = 4.75 V,	I _{OL} = 24 mA	0.35	0.5		V
I _{OZH}	Outputs	V _{CC} = 5.25 V, V _O = 2.7 V			20	μA
	I/O ports				100	
I _{OZL}	Outputs	V _{CC} = 5.25 V, V _O = 0.4 V			-20	μA
	I/O ports				-250	
I _I	V _{CC} = 5.25 V,	V _I = 5.5 V			0.1	mA
I _{IH}	V _{CC} = 5.25 V,	V _I = 2.7 V			20	μA
I _{IL}	V _{CC} = 5.25 V,	V _I = 0.4 V			-0.25	mA
I _O ‡	V _{CC} = 5.25 V,	V _O = 2.25 V	-30		-125	mA
I _{CC}	V _{CC} = 5.25 V,	V _I = 0, Outputs open		75	100	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}			R1 = 500 Ω, R2 = 500 Ω, See Figure 3	30			MHz
t _{pd}	I, I/O	O, I/O		15	25		ns
t _{pd}	CLK↑	Q		10	15		ns
t _{en}	OE↓	Q		15	20		ns
t _{dis}	OE↑	Q		10	20		ns
t _{en}	I, I/O	O, I/O		14	25		ns
t _{dis}	I, I/O	O, I/O		13	25		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

**TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2	mA
I_{OL}	Low-level output current			12	mA
f_{clock}	Clock frequency	0		25	MHz
t_w	Pulse duration, clock (see Note 2)	High	15		ns
		Low	20		
t_{su}	Setup time, input or feedback before clock↑	25			ns
t_h	Hold time, input or feedback after clock↑	0			ns
T_A	Operating free-air temperature	-55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
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electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5	V
V _{OH}	V _{CC} = 4.5 V,	I _{OH} = -2 mA	2.4	3.2		V
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4	V
I _{OZH}	Outputs	V _{CC} = 5.5 V, V _O = 2.7 V			20	μA
	I/O ports				100	
I _{OZL}	Outputs	V _{CC} = 5.5 V, V _O = 0.4 V			-20	μA
	I/O ports				-250	
I _I	Pin 1, 11	V _{CC} = 5.5 V, V _I = 5.5 V			0.2	mA
	All others				0.1	
I _{IH}	Pin 1, 11	V _{CC} = 5.5 V, V _I = 2.7 V			50	μA
	I/O ports				100	
	All others				20	
I _{IL}	I/O ports	V _{CC} = 5.5 V, V _I = 0.4 V			-0.25	mA
	All others				-0.2	
I _{OS} ‡	V _{CC} = 5.5 V,	V _O = 0.5 V	-30		-250	mA
I _{CC}	V _{CC} = 5.5 V,	V _I = 0, Outputs open		75	105	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test-equipment degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 4	25			MHz
t _{pd}	I, I/O	O, I/O			15	30	ns
t _{pd}	CLK↑	Q			10	20	ns
t _{en}	OE↓	Q			15	25	ns
t _{dis}	OE↑	Q			10	25	ns
t _{en}	I, I/O	O, I/O			14	30	ns
t _{dis}	I, I/O	O, I/O			13	30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

**TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS**

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programming information

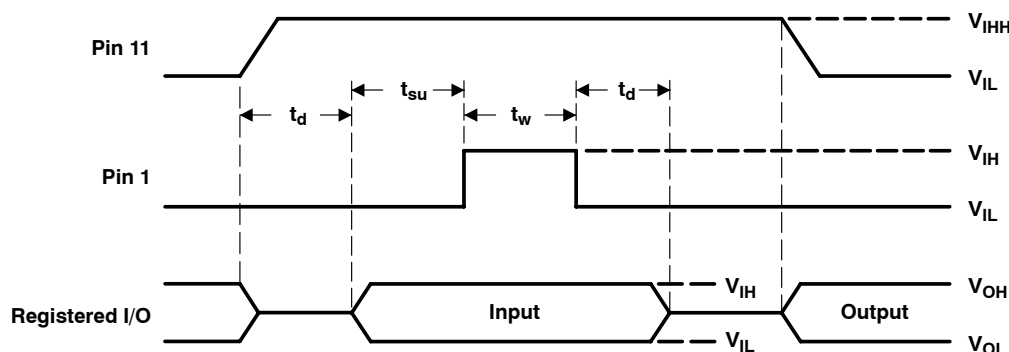
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic also is available, upon request, from the nearest TI field sales office or local authorized TI distributor, by calling Texas Instruments at +1 (972) 644-5580, or by visiting the TI Semiconductor Home Page at www.ti.com/sc.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 V and Pin 1 at V_{IL} , raise Pin 11 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 11 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.



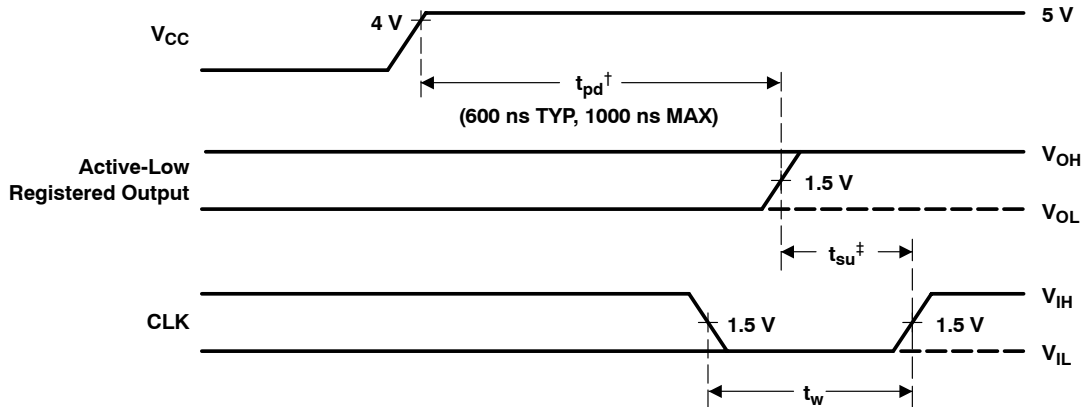
NOTE 3: $t_d = t_{su} = t_h = 100$ ns to 1000 ns $V_{IHH} = 10.25$ V to 10.75 V

Figure 1. Preload Waveforms

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
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power-up reset (see Figure 2)

Following power up, all registers are set high. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



[†] This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

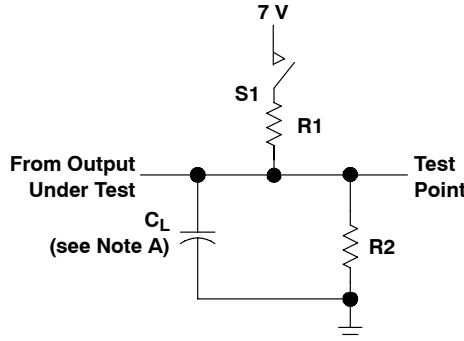
[‡] This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

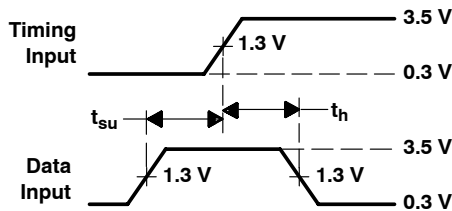
**TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS**

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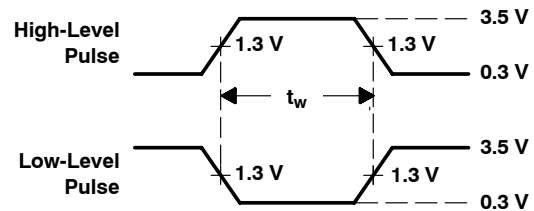
PARAMETER MEASUREMENT INFORMATION



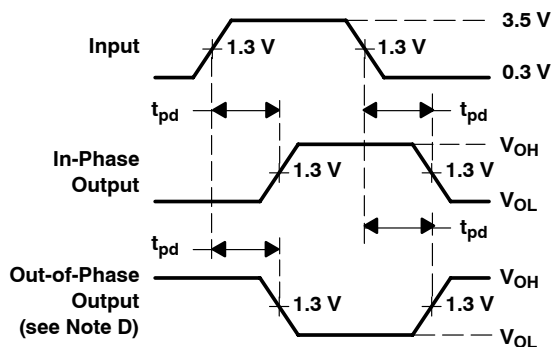
LOAD CIRCUIT FOR 3-STATE OUTPUTS



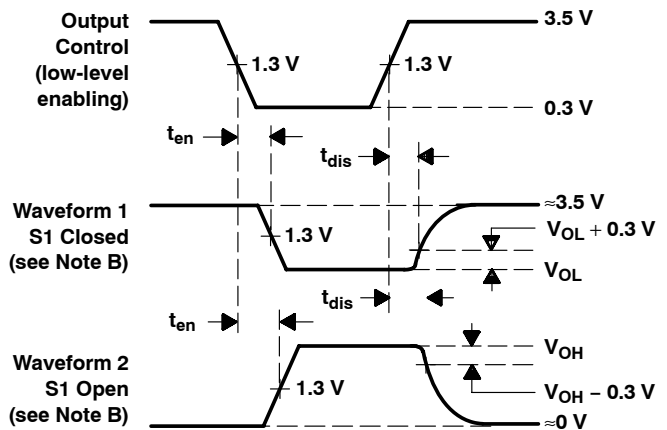
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

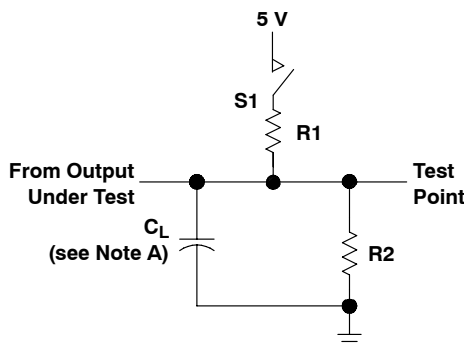
- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
 D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed. When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.
 E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

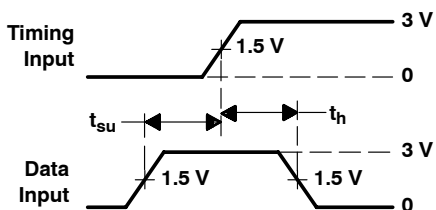
TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
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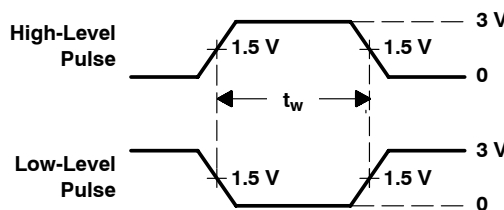
PARAMETER MEASUREMENT INFORMATION



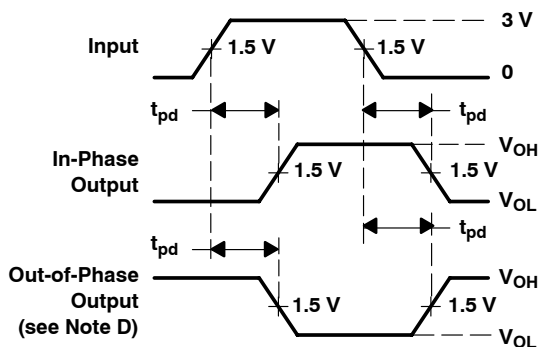
LOAD CIRCUIT FOR 3-STATE OUTPUTS



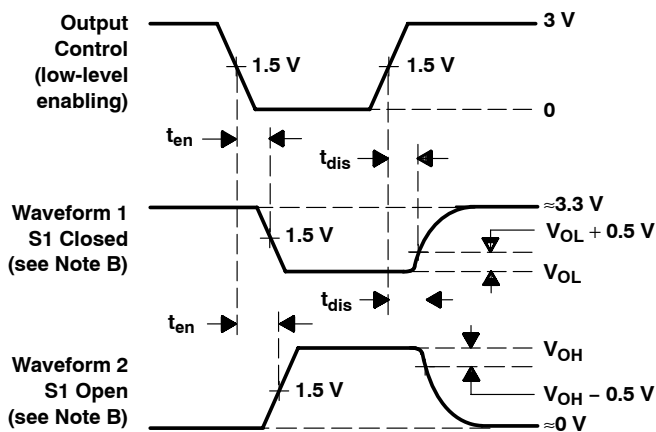
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms



PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-85155052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155052A TIBPAL16 L8-30MFKB	Samples
5962-8515505RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515505RA TIBPAL16L8-30M JB	Samples
5962-8515505SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515505SA TIBPAL16L8-30M WB	Samples
5962-85155062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155062A TIBPAL16 R8-30MFKB	Samples
5962-8515506RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515506RA TIBPAL16R8-30M JB	Samples
5962-8515506SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515506SA TIBPAL16R8-30M WB	Samples
5962-85155072A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155072A TIBPAL16 R6-30MFKB	Samples
5962-8515507RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515507RA TIBPAL16R6-30M JB	Samples
5962-8515507SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515507SA TIBPAL16R6-30M WB	Samples
5962-85155082A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155082A TIBPAL16 R4-30MFKB	Samples
5962-8515508RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515508RA TIBPAL16R4-30M JB	Samples



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8515508SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515508SA TIBPAL16R4-30M WB	Samples
JM38510/50605BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50605BRA	Samples
JM38510/50606BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50606BRA	Samples
JM38510/50607BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50607BRA	Samples
JM38510/50608BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50608BRA	Samples
M38510/50605BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50605BRA	Samples
M38510/50606BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50606BRA	Samples
M38510/50607BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50607BRA	Samples
M38510/50608BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50608BRA	Samples
TIBPAL16L8-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16L8-25	Samples
TIBPAL16L8-25CJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI			
TIBPAL16L8-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16L8-25C N	Samples
TIBPAL16L8-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155052A TIBPAL16 L8-30MFKB	Samples
TIBPAL16L8-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	TIBPAL16L8-30M J	Samples
TIBPAL16L8-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515505RA TIBPAL16L8-30M JB	Samples
TIBPAL16L8-30MWB	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515505SA TIBPAL16L8-30M WB	Samples



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIBPAL16R4-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16R4-25	Samples
TIBPAL16R4-25CJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI			
TIBPAL16R4-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16R4-25C N	Samples
TIBPAL16R4-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155082A TIBPAL16R4-30MFKB	Samples
TIBPAL16R4-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	TIBPAL16R4-30M J	Samples
TIBPAL16R4-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515508RA TIBPAL16R4-30M JB	Samples
TIBPAL16R4-30MWB	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515508SA TIBPAL16R4-30M WB	Samples
TIBPAL16R6-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16R6-25	Samples
TIBPAL16R6-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16R6-25C N	Samples
TIBPAL16R6-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155072A TIBPAL16R6-30MFKB	Samples
TIBPAL16R6-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	TIBPAL16R6-30M J	Samples
TIBPAL16R6-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515507RA TIBPAL16R6-30M JB	Samples
TIBPAL16R6-30MWB	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515507SA TIBPAL16R6-30M WB	Samples
TIBPAL16R8-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16R8-25	Samples
TIBPAL16R8-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16R8-25C N	Samples



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIBPAL16R8-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155062A TIBPAL16R8-30MFKB	Samples
TIBPAL16R8-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515506RA TIBPAL16R8-30MJB	Samples
TIBPAL16R8-30MWB	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515506SA TIBPAL16R8-30MWB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



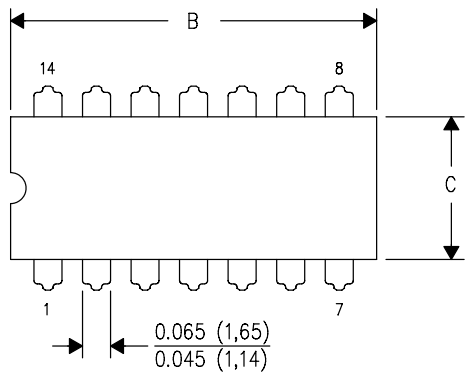
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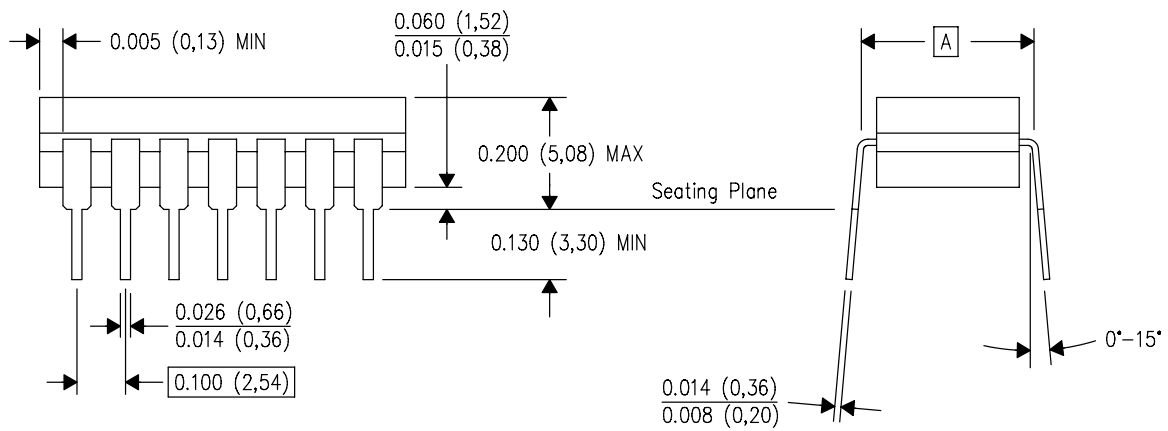
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



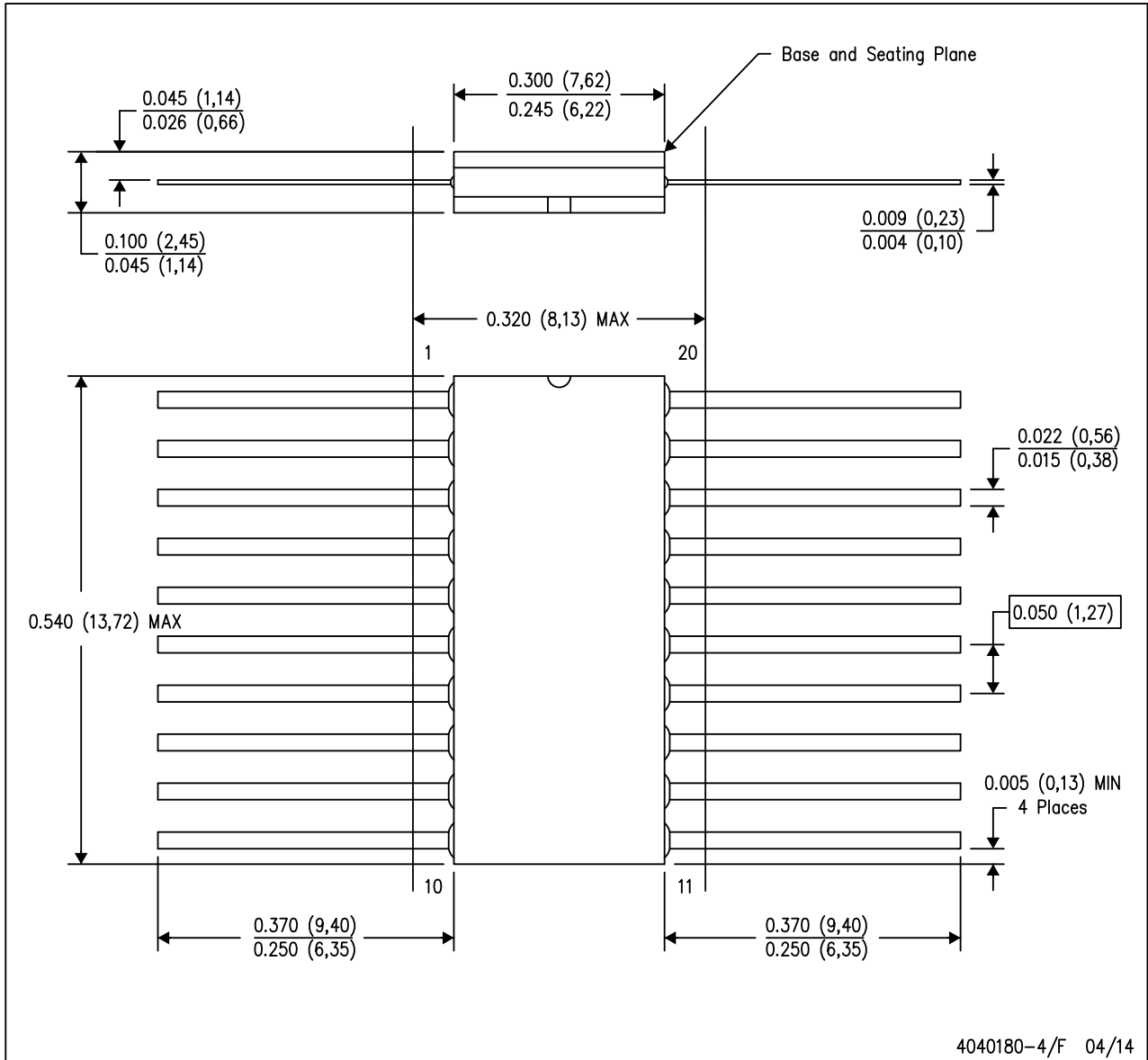
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



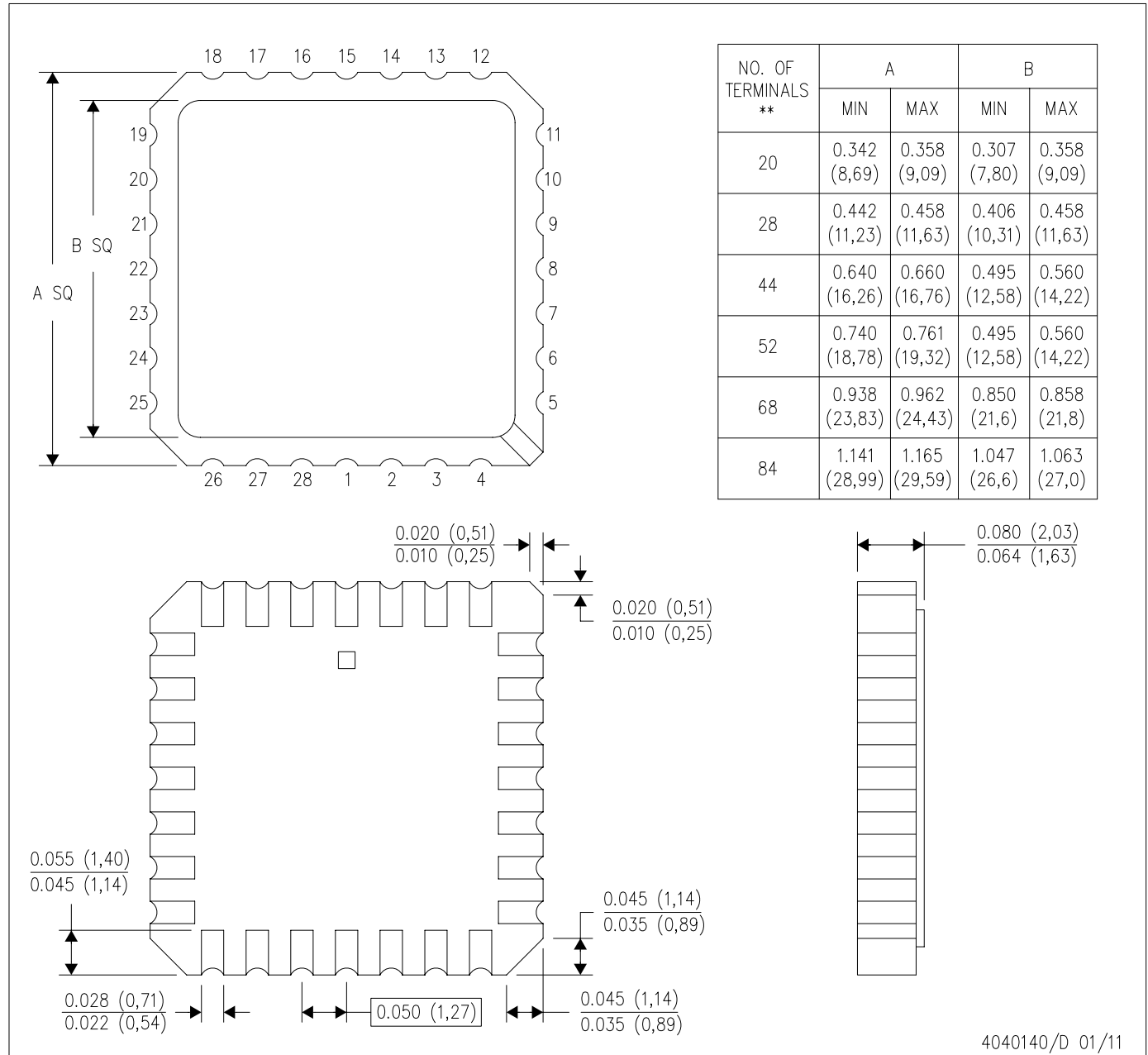
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

MECHANICAL DATA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 01/11

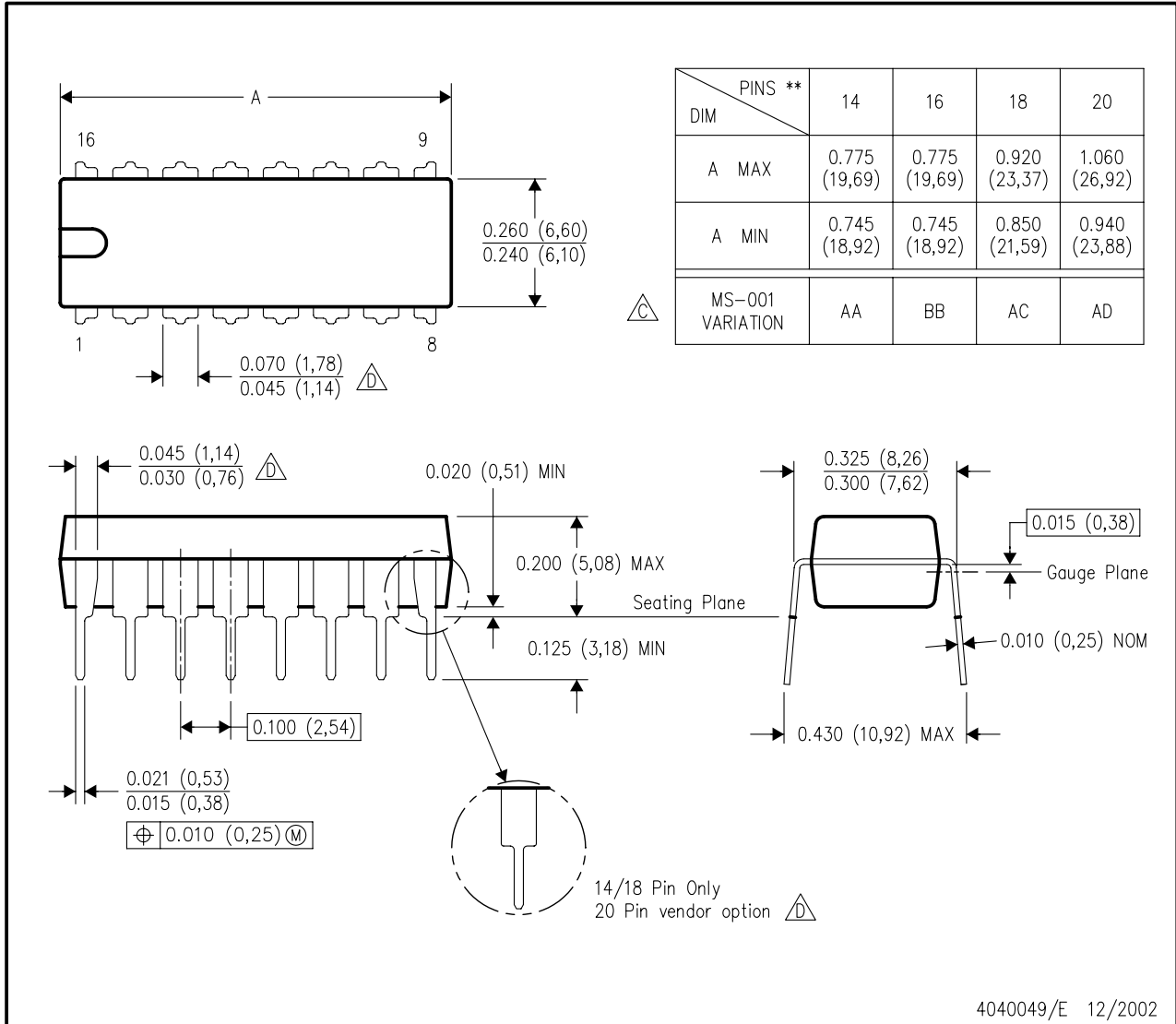
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004



MECHANICAL DATA

N (R-PDIP-T)**

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



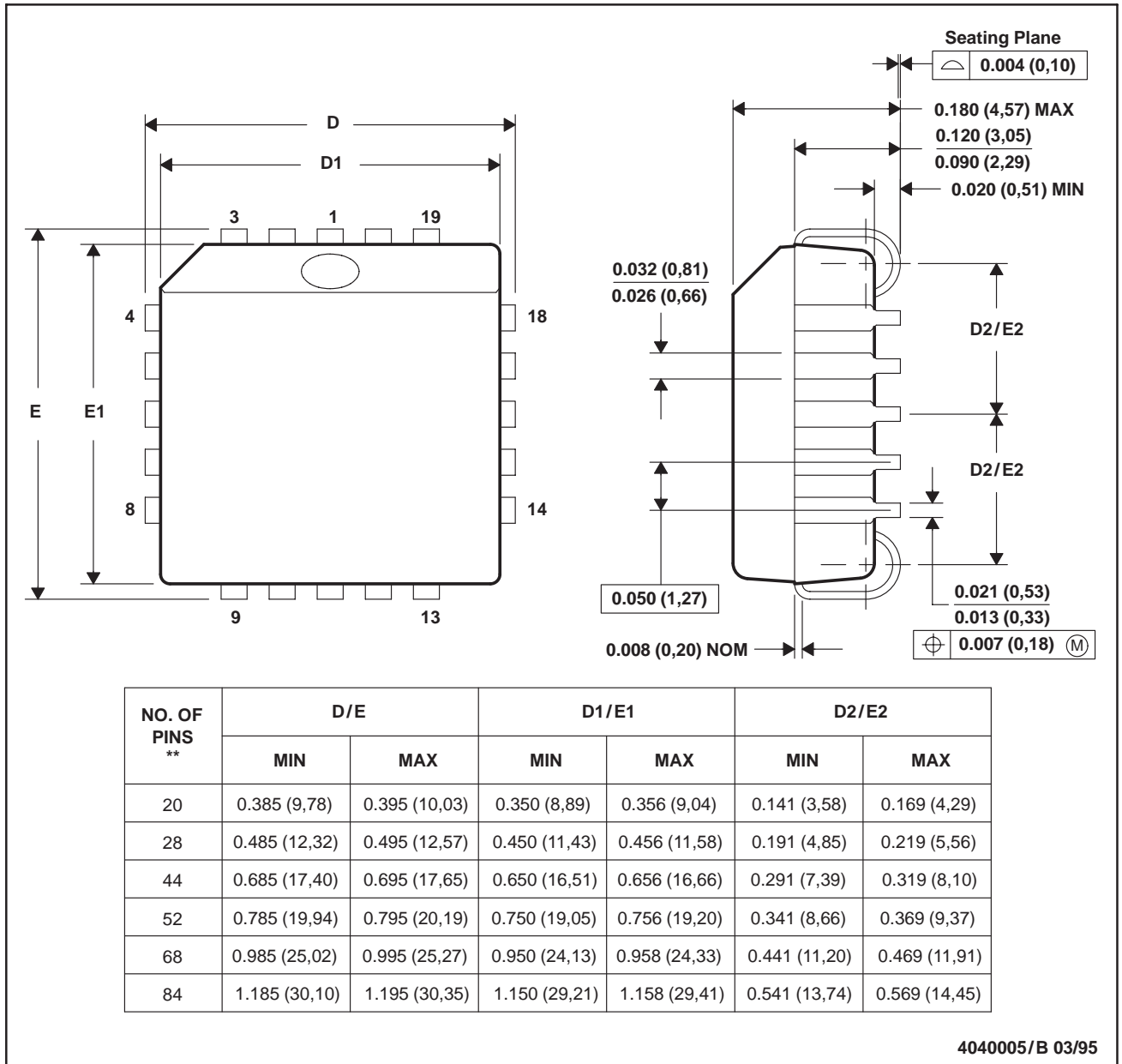
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

MPLC004A – OCTOBER 1994

FN (S-PQCC-J)**
20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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